2.830J / 6.780J / ESD.63J Control of Manufacturing Processes (SMA 6303)
Spring 2008

Control of Manufacturing Processes

Subject 2.830/6.780/ESD.63

Spring 2008

Lecture #10

Yield Modeling

March 11, 2008

References

- G. May and C. Spanos, *Fundamentals of Semiconductor Manufacturing and Process Control*, Chapter 5: Yield Modeling (Wiley 2006).
- D. J. Ciplickas, X. Li, and A. J. Strojwas, "Predictive Yield Modeling of VLSIC's," *International Workshop on Statistical Metrology,* June 2000.
- C. H. Stapper and R. J. Rosner, "Integrated Circuit Yield Management and Yield Analysis: Development and Implementation," *IEEE Trans. on Semicond. Manuf.,* Vol. 8, No. 2, May 1995.

Types of Yield-Related Problems

- Parametric failures
  - deviations in control (e.g. line width) result in functional failures or quality-loss performance degradation
- Random failures
  - uncorrelated random failure in some element
  - example: individual via failures
- Area dependent failures
  - failures related to the area of opportunity for failure
  - example: “killer defect” particles

An Integrated Circuit (IC) Yield Tree

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Particles, Defects, and Yield

- Particles are foreign matter on the surface of or embedded within the wafer
- A defect is any artifact that might destroy functionality of the circuit (particles are one type of defect)
- Functional yield can be reduced by defects
  - open circuits
  - short circuits
  - impact device operation such that function fails

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Some IC Yield Terminology

- ***Wafer yield*:** the percentage of wafers that make it to final probing
- ***Probe testing yield*:** the percentage of wafers that make it through the probe testing steps
- ***(Functional) die yield*:** the percentage of chips that make it through a functional electrical testing step (i.e. binary yes/no decision on function)
- ***Parametric (die) yield:*** the percentage of chips meeting performance specifications (e.g. speed)

Manufacturing Process Flow from the Perspective of Yield Monitoring and Control

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Statistical Basis for Yield Modeling

- The probabilities of discrete failures are generally *not* Gaussian
  - Basis in binomial and Poisson statistics

- Failure probabilities can be *spatial* in nature
  - Opportunities for failure depend on areas

Review – Binomial Distribution

- Repeated random Bernoulli trials
  - *n* is the number of trials
  - *p* is the probability of "success" on any one trial
  - *x* is the number of successes in n trials

$$f(x,p,n) = \left(\begin{array}{c} n \\ x \end{array} \right) p^x (1-p)^{n-x}, \quad x = 0, 1, 2, ..., n$$

where $\left(\begin{array}{c} n \\ x \end{array} \right)$ is "n choose x" $= \frac{n!}{x!(n-x)!}$

$$\mu = np$$
$$\sigma^2 = np(1-p)$$

- Yield application
  - probability of *x* good chips on a wafer with *n* chips, given probability any given chip is good

Review – Poisson Distribution

$$f(x,\lambda) = \frac{e^{-\lambda}\lambda^{x}}{x!}, \quad x = 0, 1, 2, ... \qquad\qquad x \sim P(\lambda)$$

- Mean: $\mu = \lambda$
- Variance: $\sigma^2 = \lambda$
- Example applications:
  - # misprints on page(s) of a book
  - # transistors which fail on first day of operation
- Poisson is a good approximation to Binomial when *n* is large and *p* is small (< 0.1)

$$\mu = \lambda \approx np$$

Example: Via Yield

- Chips have multiple wiring layers with *vias* between layers
  - Very small failure probability p_v for any one via.
  - Millions of vias in each layer on each chip, i.e. n is large.
- Statistical Model?
  - Could use a binomial distribution to find the probability there will be some number x of via failures on the chip
  - Alternatively, can use a *failure rate* (or average number of via failures) $\lambda_v \simeq np_v$ for vias on a layer. Now the probability of x via failures on some chip is approximated by a Poisson distribution:

$$f(x, \lambda_v) = \frac{e^{-\lambda_v} \lambda_v^x}{x!}, \quad x = 0, 1, 2, ...$$

  - Assuming that *all* vias must work correctly for the chip to work, (i.e. $x = 0$), what is the probability that the chip is good?

$$\Pr(\text{chip good}) = f(0, \lambda_v) = e^{-\lambda_v}$$

Binomial vs. Poisson Distribution

- Comparison between approximations of the binomial and Poisson distributions:

$$B(x, p_v, n) = \left(\begin{array}{c} n \\ x \end{array} \right) p_v^x (1-p_v)^{n-x}, \quad x = 0, 1, 2, ..., n$$

$$\begin{aligned} B(0, p_v, n) &= \left(\begin{array}{c} n \\ 0 \end{array} \right) p_v^0 (1-p_v)^{n-0} \\ &= (1-p_v)^n \approx 1 - np_v \quad \text{for small } p_v \end{aligned}$$

$$P(x, \lambda_v) = \frac{e^{-\lambda_v} \lambda_v^x}{x!}, \quad x = 0, 1, 2, ...$$

$$P(0, \lambda_v) = e^{-\lambda_v} \approx 1 - \lambda_v \quad \text{for small } \lambda_v$$

$$\lambda_v = np_v$$

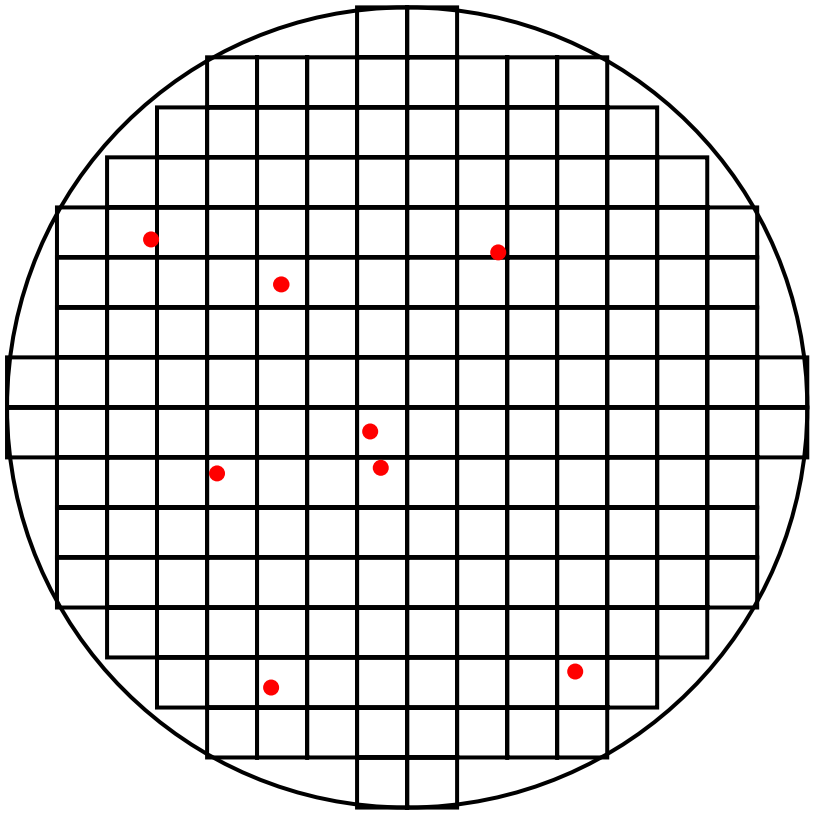
Defect (Spatial) Yield Modeling

$$Y = f(A_0, D_0)$$

- D_0 – average number of defects per unit area
- A_0 – the critical area of the system (the area in which a defect occurring has a high likelihood of causing a fault)

May & Spanos

Spatial Defects



- Random distribution
- Spatially uncorrelated
- Each defect “kills” one chip

Empirical Result: Exponential Dependence of Yield on Chip Area

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Poisson Defect Yield Model

- Assumptions
  - defects are “points”
  - every defect results in a fault
  - defects are spatially uncorrelated
- Then yield of any given circuit with critical area A_c and defect density D_0 is

$$Y = e^{-A_c D_0}$$

- And for a chip with N circuits each with critical area A_c, yield is

$$Y = e^{-N A_c D_0} = e^{-A_0 D_0}$$

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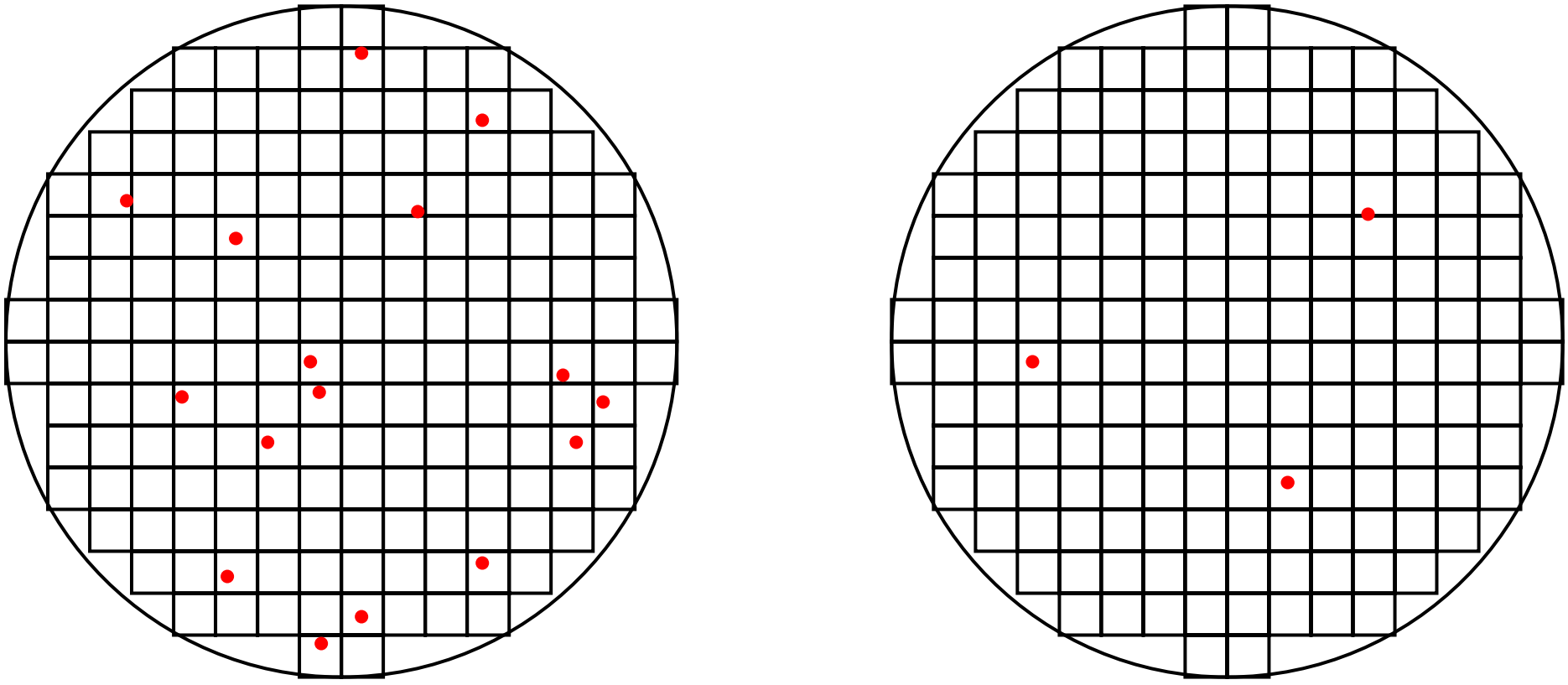
Murphy Yield Model



- Wafers will experience different defect densities
  - pdf associated with defect density

Murphy Yield Model

- Observation:
  - Value of defect density is not a constant
  - Rather, there is a pdf associated with finding different defect densities
- Thus $$Y = \int_0^\infty e^{-A_0 D} f(D) dD$$
- Poisson yield model is special case, assumes

$$f(D) = \delta(D - D_0)$$

$$Y_{\text{poisson}} = e^{-A_0 D_0}$$

May & Spanos

Murphy Yield Model, p. 2

- Murphy considered different *f(D)* distributions
- A **uniform** *f(D)* results in

$$Y_{\text{unif}} = \frac{1-e^{-2A_0D_0}}{2D_0A_0}$$

- A **gaussian** *f(D)* not integrable in closed form
- A **triangular** *f(D)* results in

$$Y_{\text{tri}} = \left(\frac{1-e^{-A_0D_0}}{D_0A_0}\right)^2$$

May & Spanos

Seeds Yield Model

- Seeds proposed an exponential defect density distribution:
  - high yield occurs when have large proportion of low defect densities and a small proportion of high defect densities

$$f(D) = \frac{1}{D_0} \exp\left(\frac{-D}{D_0}\right)$$

  - gives a yield expression:

$$Y_{\text{exp}} = \frac{1}{1+D_0 A_0}$$

May & Spanos

Comparison of Defect Density Models

Poisson

Uniform

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May & Spanos

Triangular

Exponential

Negative Binomial Model

- Gamma probability distribution for *f(D)*
  - proposed by Ogabe, Nagata, and Shimada; popularized by Stapper

$$f(D) = \frac{D^{\alpha-1} e^{-D/\beta}}{\Gamma(\alpha)\beta^{\alpha}}$$

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- α is a "cluster" parameter
  - High α means low variability of defects (little clustering)
- Resulting yield:

$$Y_{\text{gamma}} = \left(1 + \frac{A_0 D_0}{\alpha}\right)^{-\alpha}$$

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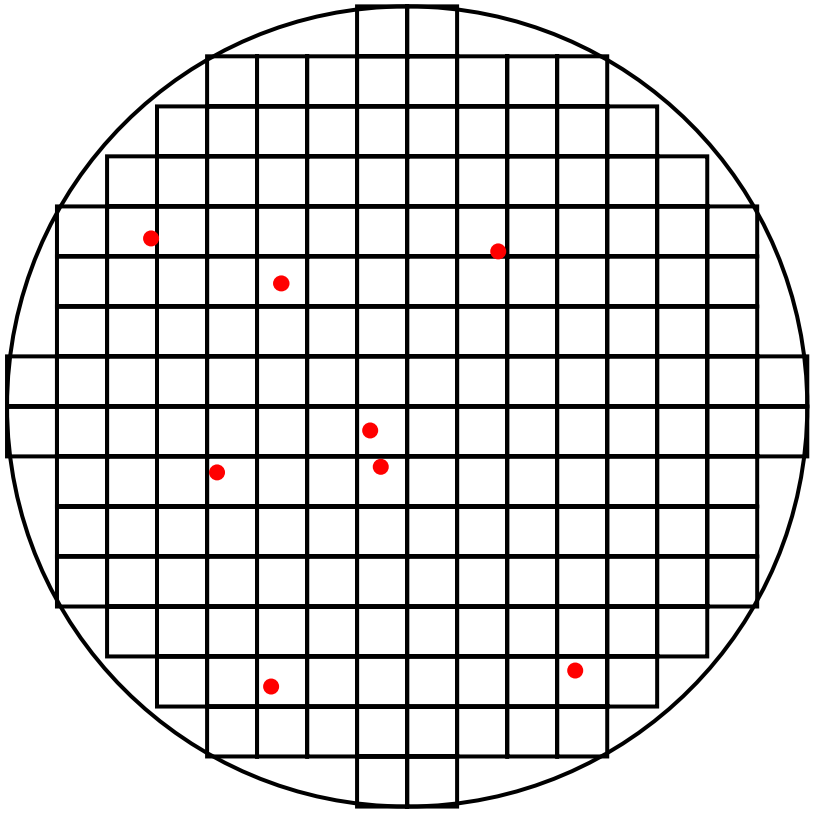
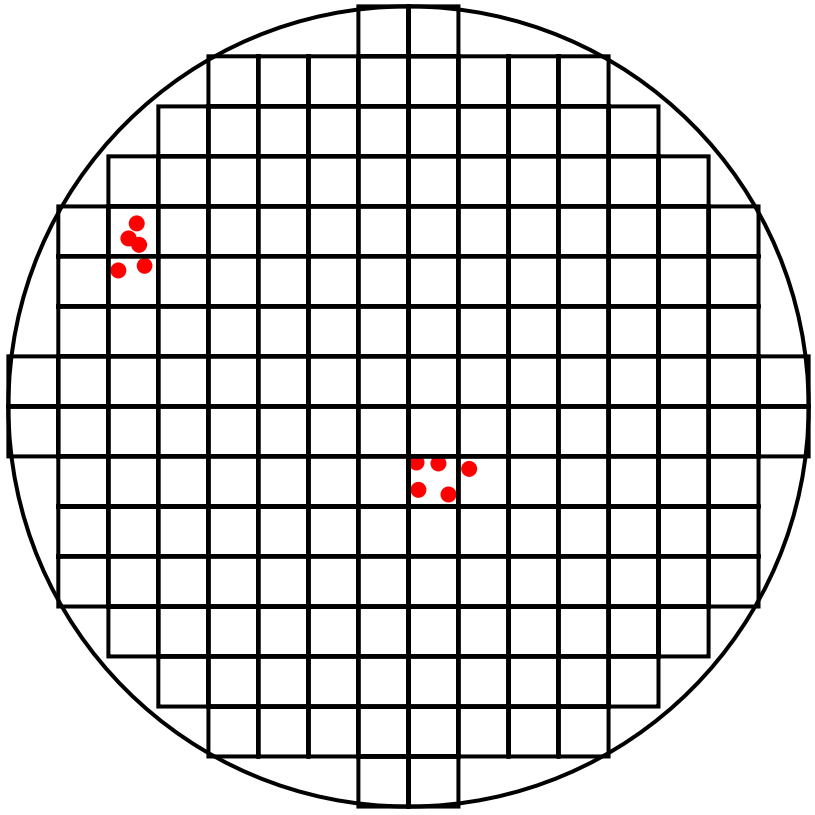
Spatial Defects



- Random distribution
- Spatially uncorrelated
- Each defect “kills” one chip



- Spatially clustered
- Multiple defects within one chip (can’t already kill a dead chip!)

Negative Binomial Model, p. 2

- Large α limit (little clustering)
  - gamma density approaches a delta function, and yield approaches the Poisson model:

$$Y = \lim_{\alpha \to \infty} \left(1 + \frac{A_0 D_0}{\alpha}\right)^{-\alpha} = \exp(-A_0 D_0)$$

- Small α limit (strong clustering)
  - yield approaches the Seeds model:

$$Y = \lim_{\alpha \to 0} \left(1 + \frac{A_0 D_0}{\alpha}\right)^{-\alpha} = \frac{1}{1 + A_0 D_0}$$

- Must empirically determine α
  - typical memory and microprocessors: α = 1.5 to 2

How About Size of Defects?

- So far we've talked about *f(D)* – the probability distribution function for the number ***density*** (average number per unit area) of defects

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- Also characterize the ***sizes*** of defects
  - important factor in whether or not a *fault* (functional failure) will occur:
  - interacts with our notion of ***critical area***

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Defect Size Distribution

- Empirical results suggest a power law for the distribution of defect sizes: $D(x) = \frac{N}{x^p}$
  - *x* is the defect size (diameter assuming spherical defects)
  - *N* is a technology parameter
  - *p* is an empirical parameter
- Assumes defects are located randomly across wafer
  - Average defect density D_0 is then related to the defect size
  - x_0 is the minimum defect size ($\approx$ min feature size)

$$\begin{aligned} D_0 &= N \int_{x_0}^{\infty} D(x)dx \\ &= N \int_{x_0}^{\infty} \frac{1}{x^p} dx \\ &= \frac{N}{1-p}\left(1 - {x_0}^{1-p}\right) \end{aligned}$$

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Critical Area

- Not all parts of layout are equally likely to fail due to presence of defects
- For a given defect size (assume circular shape), we can calculate the area of the layout where the center of that defect must fall in order to cause a failure
  - may have a critical area for open faults
  - may have a different critical area for shorts

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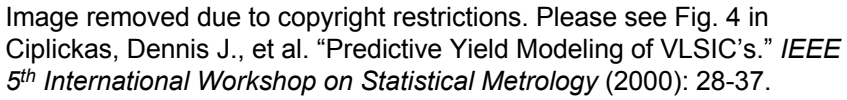
Measurement & Defect Size Distribution



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Measurement:

- Can be difficult: minimum feature may be smaller than size of defects that can be easily measured
- Approach: apply scaling function *f(x)* to correct for size and measurement interactions

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How Measure Defect Size Distribution?

- Electrical test
  - measure shorts in test structures for different spacings between patterned lines (at or near the “design rule” or DR feature size)
  - measure opens in other test structures

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“Nest” structure

Hess, ISQED 2003 Tutorial

Critical Area

- Can define critical area A_0 as: *May & Spanos*

$$A_0 = A \int_{x_0}^{\infty} POF(x) D(x) dx$$

- where
  - A is the chip area
  - x_0 is min defect size
  - $D(x)$ is the defect size distribution
  - $POF(x)$ is probability of failure (which depends on the feature size)

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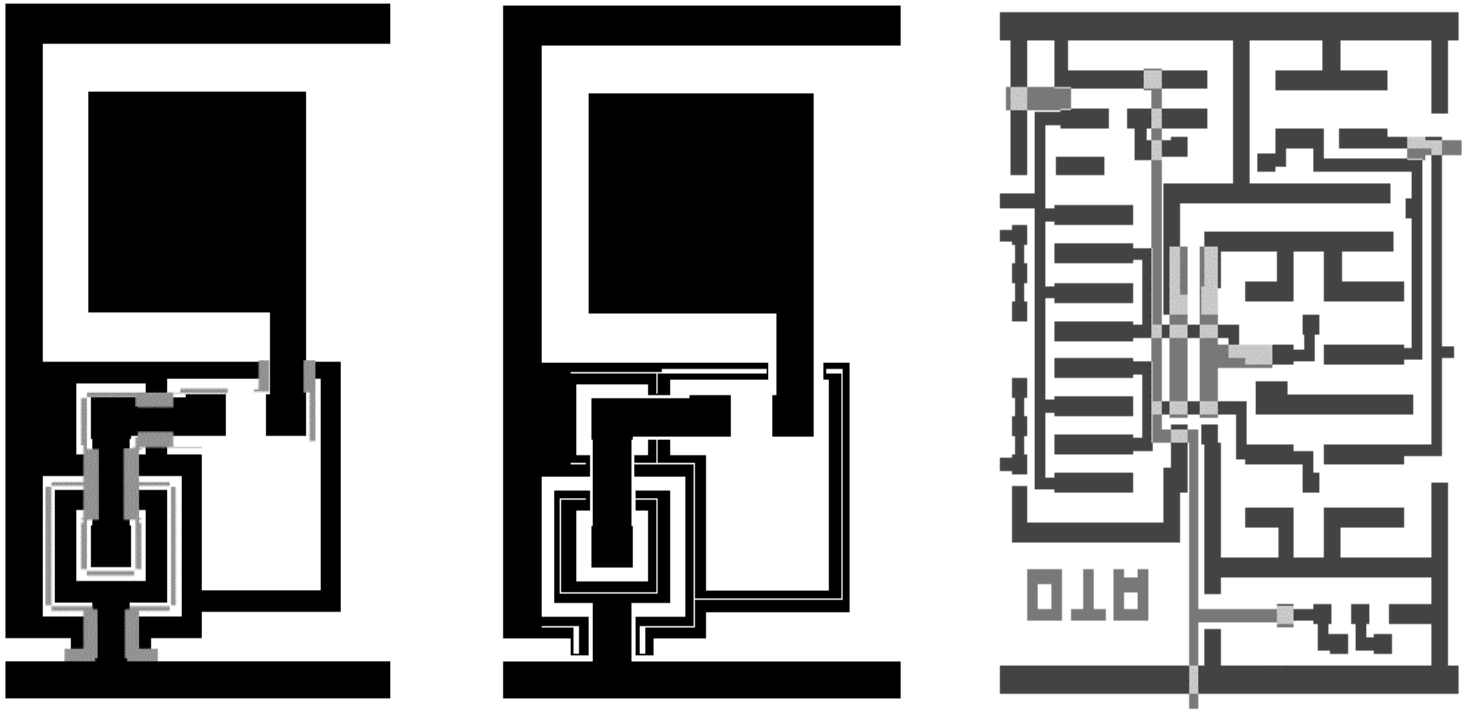
Critical Area Extraction

- A variety of tools to examine a layout and calculate critical areas for different types of faults

Shorts **Breaks** **Vertical Shorts**



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Stamenković, ISQED 2003 Tutorial

Putting Critical Area and Defect Size Distribution Together

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- For small defects, yield impact is small (critical area is small)
- For large defects, yield impact is small (very few large defects)
- Key area: defects near minimum feature size on layout

Global Yield Loss

- Previous discussion focused on *local* defects (e.g. particles)
- *Global defects* may also exist
  - typically spatially correlated
  - due to process fluctuations
  - may have a clear spatial pattern
- Account for with a global factor Y_0
  - Y_0 not related to defect density or critical area

$$Y = Y_0 \left(1 + \frac{A_0 D_0}{\alpha}\right)^{-\alpha}$$

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Chip Yield

- *MANY* opportunities for yield loss
  - some patterned layers are sensitive to defect/particle yield loss
  - some patterned layers are sensitive to random yield loss
  - different regions on the chip (with different layout characteristics) will be differently susceptible to defects
- Can build a yield impact matrix
  - calculate partial yield for each block on chip, for each layer

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Chip Yield

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- "Limited Yield"
  - loss from different layers, for each block
  - can consider DFM changes to improve yield (e.g. wider spacing)

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Characterization Vehicles (Test Chips)

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Summary

- **Functional Yield:** complex parts (e.g. ICs) require large numbers of subcomponents to all function
  - Random defects can cause failure
  - Spatial defects (e.g. particles) can cause failure
- **Parametric Yield:** deviations from designed dimensions, material properties can also cause failure or performance/quality loss
- **Approach:** Modeling of
  - Defect density distribution *f(D)*
  - Defect size distribution *D(x)*
  - Critical area as a function of defect size $A_0(x)$
  - Integrated yield impact, across multiple layers and IC blocks