6.896
4.7-2004
L15.1
Bradley C Kuszmaul

"VLSI"

Now we switch gears + talk about the physical design of circuits. Circuits take area on a chip, or volume in a computer. ~~The goal is to deep analyse circuits,~~ We can analyse circuits for their area just like for their time.

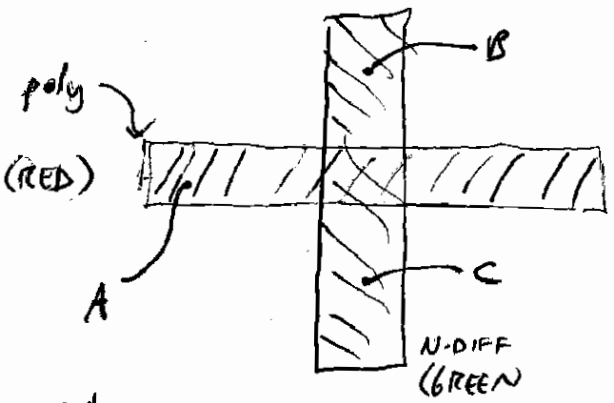
VLSI circuits are drawn with rectangles

Sidebar: ~~Rectangles~~ Color Code

polysilicon — RED
N-diffusion — ~~RED~~ GREEN
~~P-diff~~ — YELLOW (WHITE)

<MAGIC>

use MAGIC colors



When you cross green + red you get a transistor.

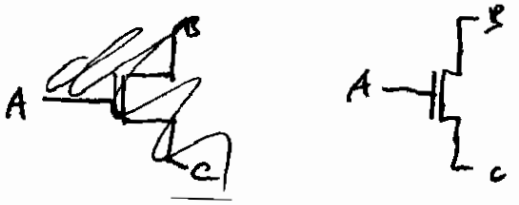
Metal
Oxide
Semiconductor
Field
Effect
Transistor

~~Three regions~~:
~~A = all red~~
~~B = green on top of red~~
~~C = green below red~~

This is an N-FET because it uses N-diffusion

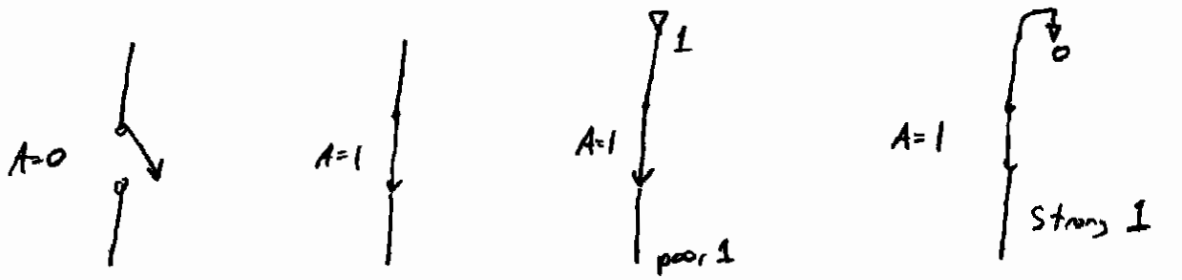
3 Regions:
A - all red area
B = green ~~and~~ above red
C = green below red

In schematic this is



6.896 4-7-04 L5.2

N-FET behavior: (A switch)



switch open

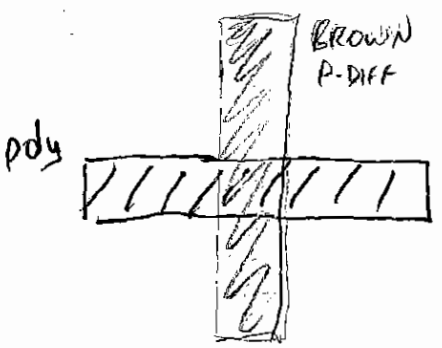
switch closed

But the ~~bubble~~ N-FET is only good at transmitting 0's.

P-FET

Could to sidebar:

P-diffusion BROWN (MAGIC)
GREEN (MOSIS)



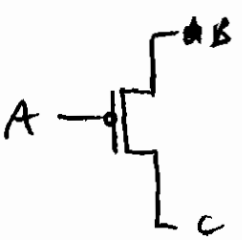
P-FET

~~Opposite behavior~~

~~A=1 open~~

A=0 ⇒ closed, passes 1's well

A=1 ⇒ open

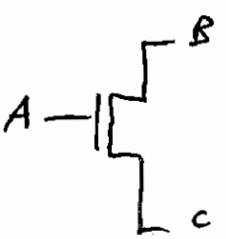


"Bubble means P-FET"
"active low"

N-FET

A=0 open

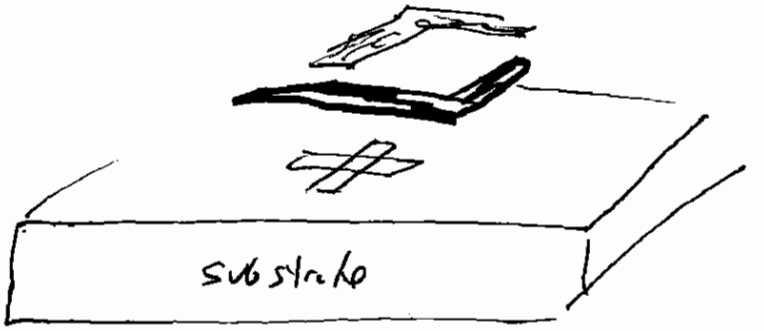
A=1 closed, passes 0's well



No bubble = NFET
"active high"

6.896 4-7-04 15.3

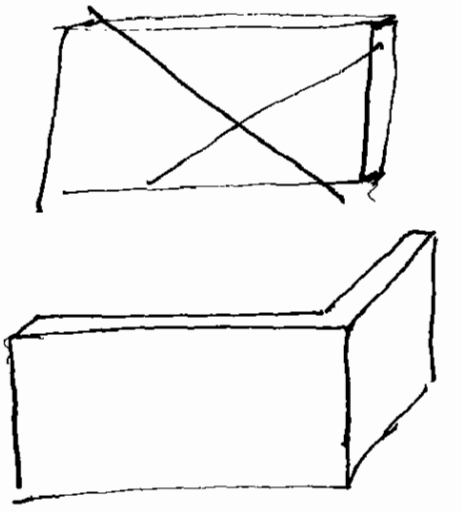
VLSI is a club sandwich



Bottom layer: substrate
next: diff-stuff + poly
next: metal 1 (blue) [add to sidebar]
next: metal 2 (purple) [add to sidebar]

Old Days:
1 or 2 layers of metal
flat wide wires

Now:
20 layers of metal
tall thin wires



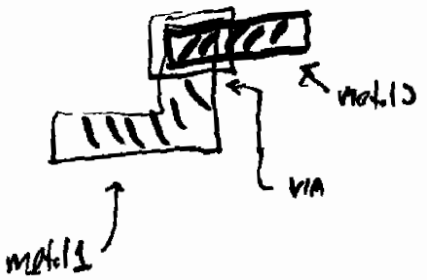
(For EE's)
Implications: in old days capacitive coupling mostly between wire + substrate. $C = O(\text{Area of rectangle})$

Now: most ~~coupling~~ coupling is between adjacent wires. $C = O(\text{Perimeter of rectangle})$

Lots of crosstalk.

6.896 4-7-04 15.4

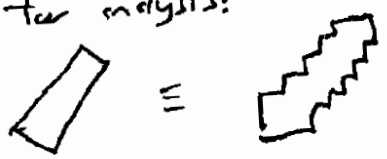
Adjacent layers connected by vias



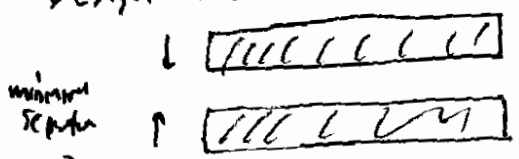
Build a 3-D maze of conductor out of metal.

Angles: We'll stick to 90° angles
Modern technologies include 45° + other angles.

Only a Constant factor for analysis:



Design Rules:

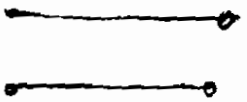


minimum line width (to avoid open circuit)

to avoid short circuit.

Can be combined to "center-to-center spacing"

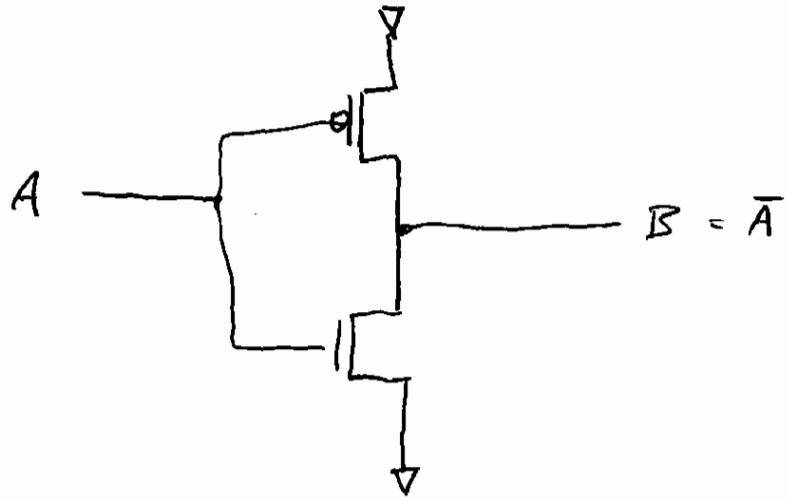
Can draw the lines on a grid, + capture all info.



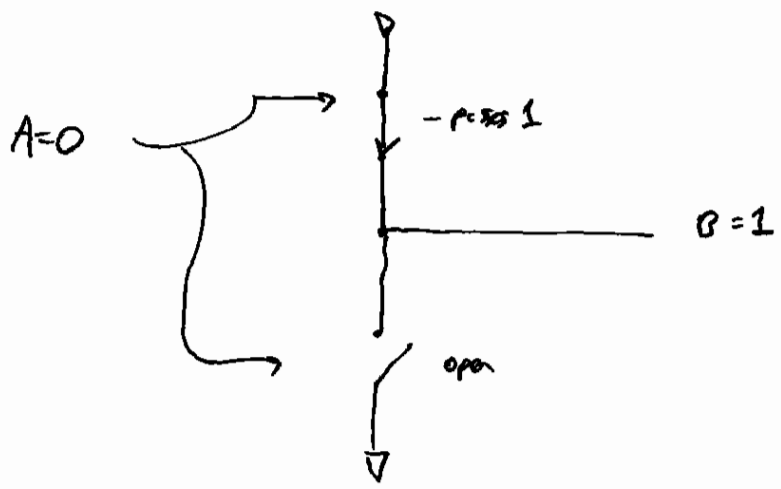
6.896 4.7-04 15.5

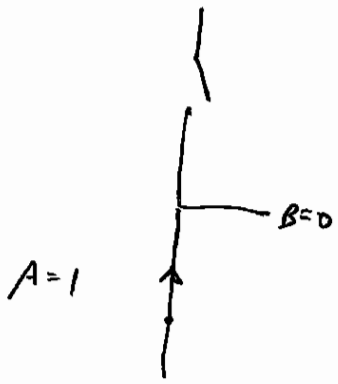
A CMOS inverter.

Schematic:



How it works

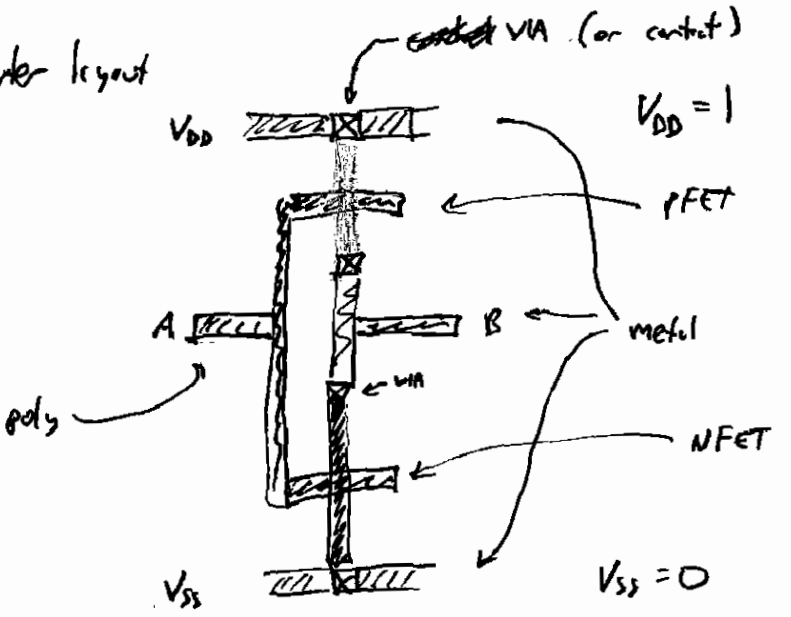




The P-FETs are used to pass 1's, the NFETs to pass 0's.

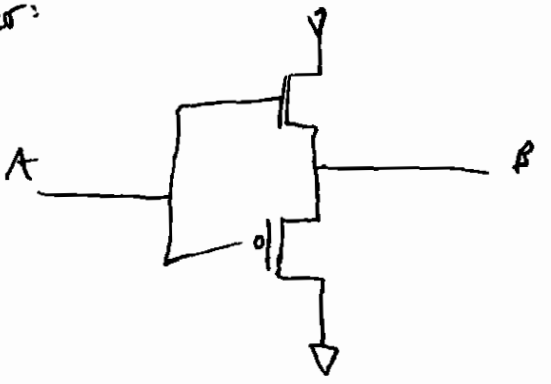
6.896 4.7-04
15.6

Inverter layout



---

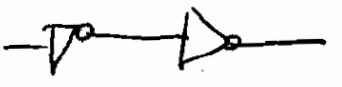
a repeater:



$B = A$

WRONG NFET can't pass a good 1

Must use two inverters



Q: Why would you want a repeater?

A: To send long distance, a repeater takes a poor 1 + restores it to a good 1.

6.896 4-7-04

15.7

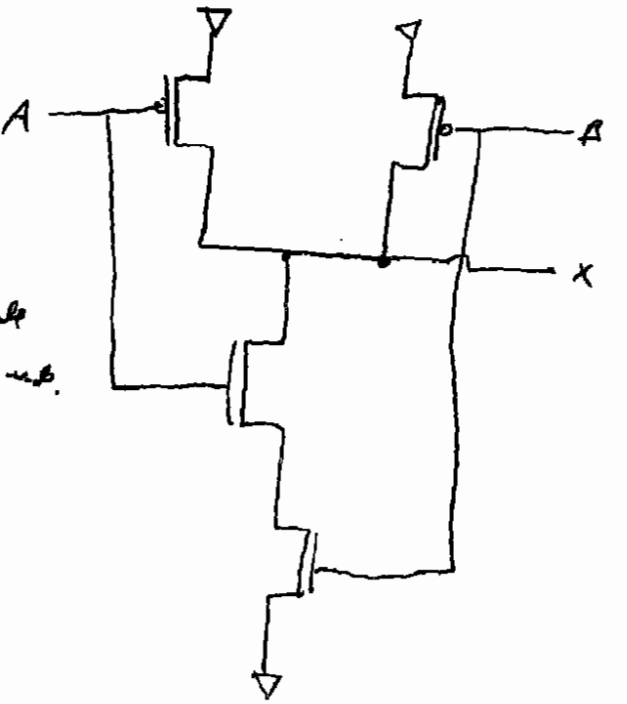
NAND GATE:

TRUTH TABLE

A	B	X
0	0	1
0	1	1
1	0	1
1	1	0

LOGIC SYMBOL

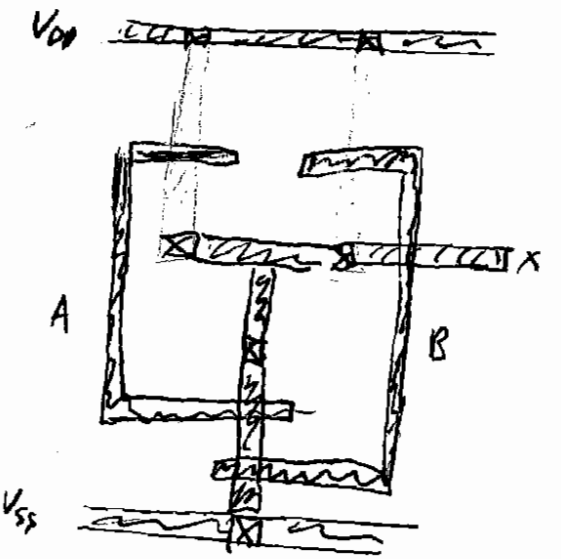
ELECTRICAL SCHEMATIC



If A or B is 0 then output to 1 will make

If A + B are both 1 then output to 0 is made.

LAYOUT



Exercise: Design + Draw a 2-input NOR gate

6.896 15.8 4.7-04

Side-Trip: De Morgan's Law

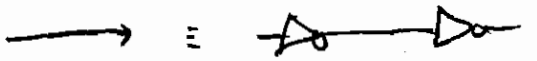
Let A be a circuit comprising inverters, wires, ORs, inputs, outputs

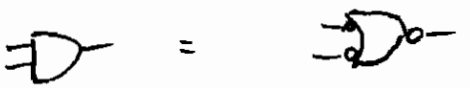
Let $\bar{A}$ be the circuit with all ANDs replaced by ORs, & all ORs replaced by ANDs.

Then if we add inverters to the inputs & outputs of $\bar{A}$ we get a circuit functionally equivalent to A [De Morgan's Law]

Proof: By induction on circuit size.

Base cases

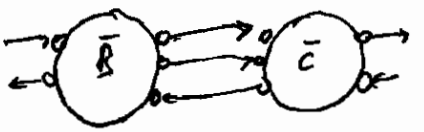




Inductive step:

A:

$\equiv$ By ind. hyp



$\equiv$ cancel

$\equiv$

6.896 4.7.04

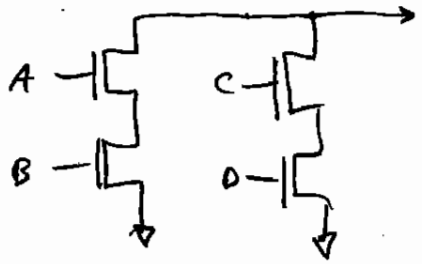
15.9

A bisser example: $F = \overline{A \cdot B + C \cdot D}$

Need: a path to 0 iff F is false
a path to 1 iff F is true

The N-side (path to 0)

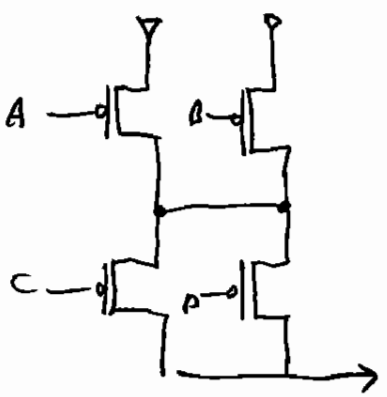
N-fets create path when $\overline{A \cdot B + C \cdot D}$ is false,
i.e. $A \cdot B + C \cdot D$ is true



The P-side: path to 1 if $\overline{A \cdot B + C \cdot D}$ is true.

Path made of P-FETS, so all inputs must be inverted to make the p-fets switch on. Use Demorgan

$$\overline{A \cdot B + C \cdot D} \equiv (\bar{A} + \bar{B}) \cdot (\bar{C} + \bar{D})$$



Exercise: Design Electrical-Level circuit for
$F = \overline{(A+B+C) \cdot D}$