Lecture 20 - The Si surface and the Metal-Oxide-Semiconductor Structure

March 22, 2007

Contents:

Reading assignment:

del Alamo, Ch. 8, §§8.1-8.2 (8.2.1-8.2.2)

Key questions

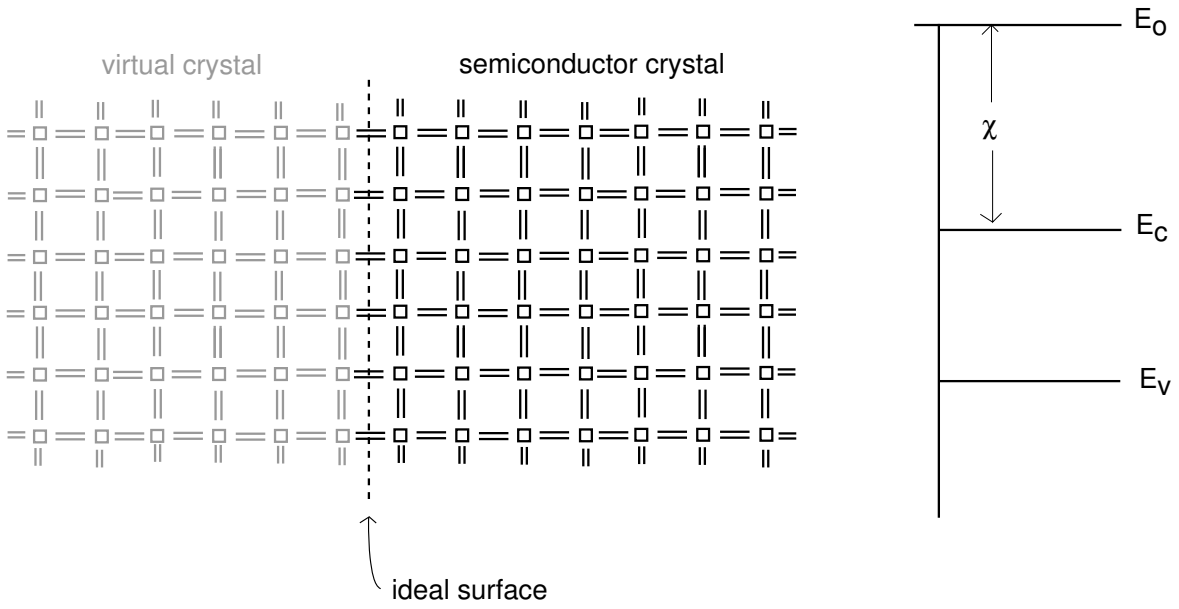
- How does the surface of a semiconductor look like at the atomic level?
- If one assembles a metal-oxide-semiconductor structure and sets it up at zero bias, what is the final situation?
- How does this picture change for different choices of metal work function?

1. Semiconductor Surface

At a surface, perfect crystalline periodicity of solid comes to an abrupt end. What happens?

□ *Ideal semiconductor surface*

Semiconductor comes to an end, but bulk properties unaffected → bonding arrangement at surface unchanged from bulk.



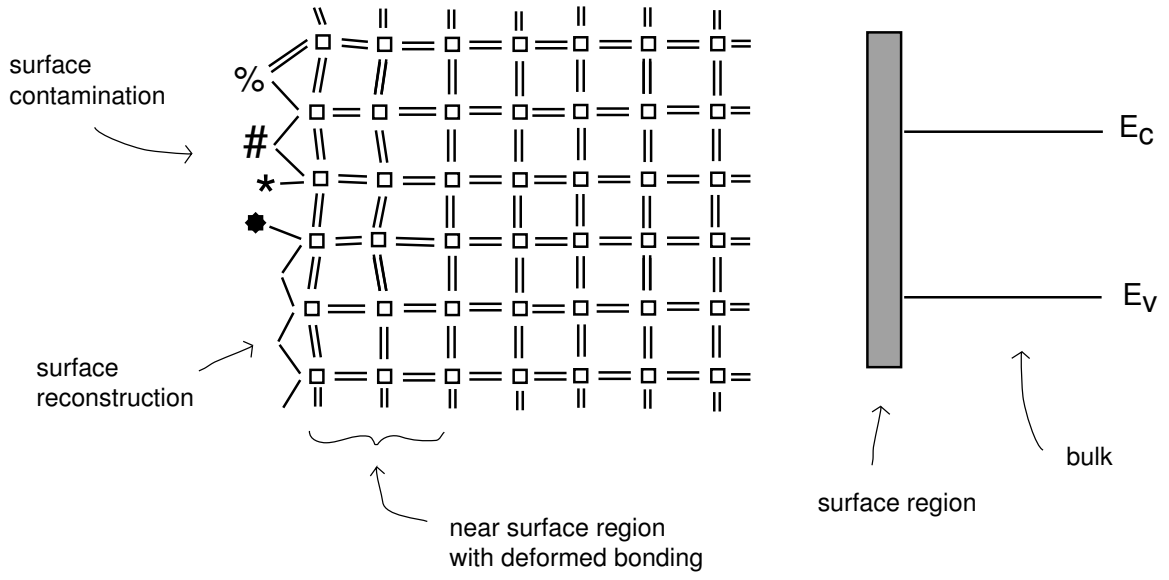
Zero carrier current normal to surface; other than that, carriers unaffected by surface.

□ *Real surface*

In ideal surface, four-fold coordination of atoms cannot be preserved ⇒ broken bonds ⇒ surface is very reactive.

Surface can lower its energy by:

- **surface contamination**: absorption of O, C, and other foreign atoms and molecules
- **surface reconstruction**: surface atoms bond among themselves.



Example of surface reconstruction: 7x7 (111) Si surface:

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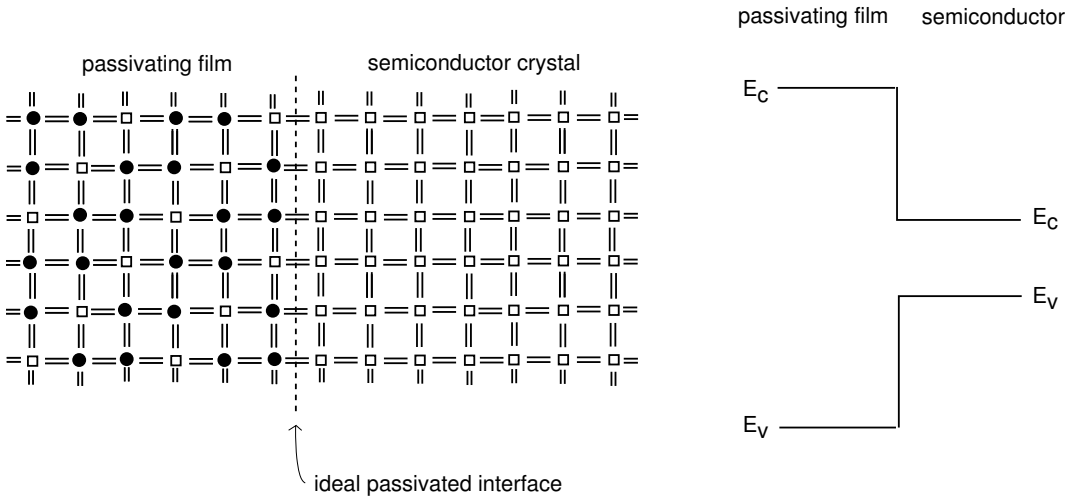
□ *Passivated surface*

"Coating" of semiconductor surface with *passivating layer* so that bulk bonding prevails for surface atoms.



Most important passivating material: SiO_2 - one of the keys of the microelectronics revolution:

- amorphous dielectric: only short-range order
- natural product of Si oxidation ("Si rusts!")
- exceptional chemistry
- nearly ideal interface with Si

Wide energy gap of SiO_2 prevents carriers from escaping from semiconductor.

Residual surface roughness in modern Si/SiO_2 structures: ~ 2 monolayers.

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Figure 1 (a) on page 246 in
Buchanan, D. A. "Scaling the Gate Dielectric: Materials, Integration and Reliability."
IBM Journal of Research and Development 43, no. 3 (1999): 245-264.

2. Ideal Metal-Oxide-Semiconductor structure at zero bias

MOS structures pervasive in modern microelectronics:

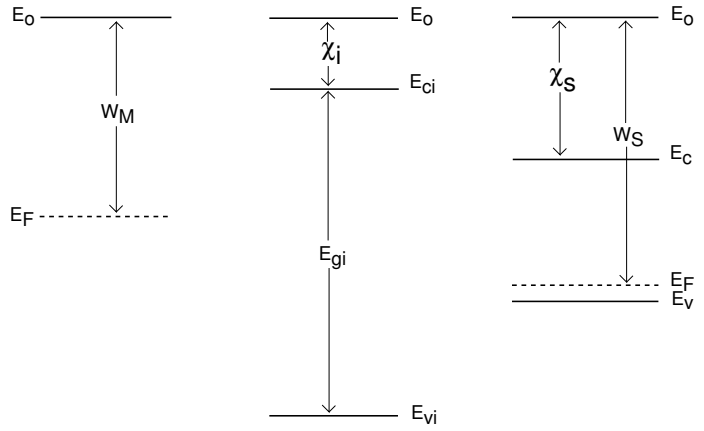
- heart of MOSFETs (from which CMOS is made)
- heart of DRAMs, Flash memories
- MOS structure everytime a metal line runs over a dielectric-coated semiconductor

MOS understanding is portable $\Rightarrow$ view it as generic sandwich of highly conducting material/dielectric/semiconductor (better name MIS)

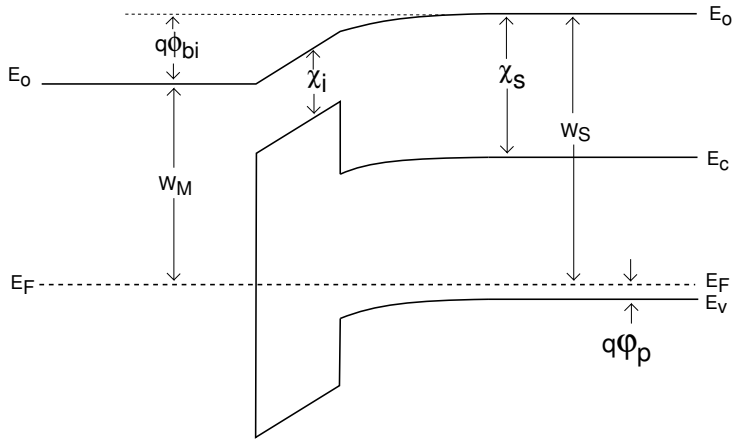
- Al/SiO_2/Si (early MOSFETs)
- n^+-polySi/SiO_2/Si (modern MOSFETs)
- Al/Si_3N_4/Si (metal lines on Si)
- WSi/AlGaAs/InGaAs (modern high-frequency transistors)

□ *Energy band diagram* (p-type substrate)

Insulator does not allow charge exchange between metal and semiconductor ⇒ thermal equilibrium not well defined, need wire that connects metal and semiconductor: talk about *zero bias*.



a) metal, insulator and semiconductor far apart

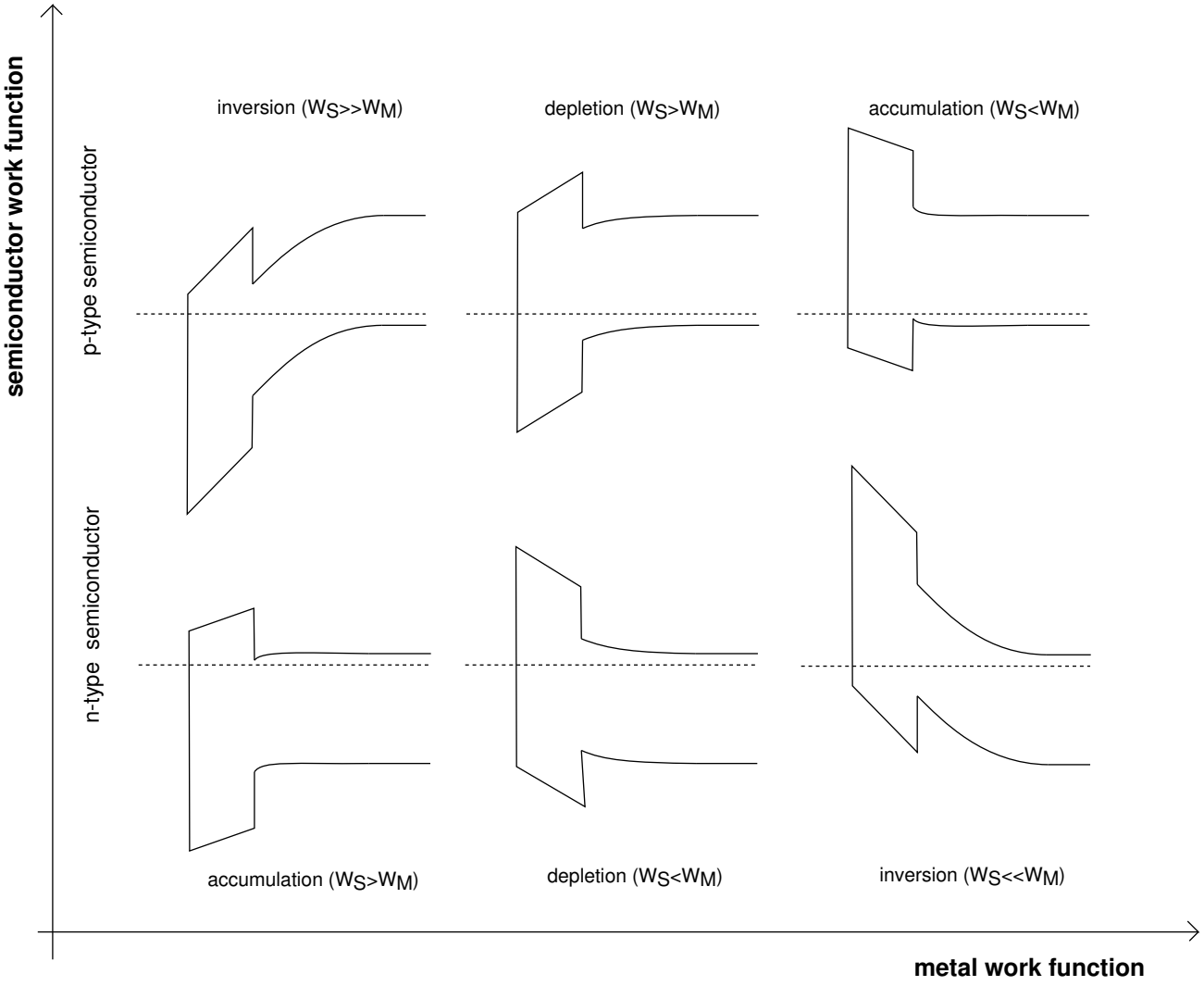


b) metal, insulator and semiconductor in intimate contact

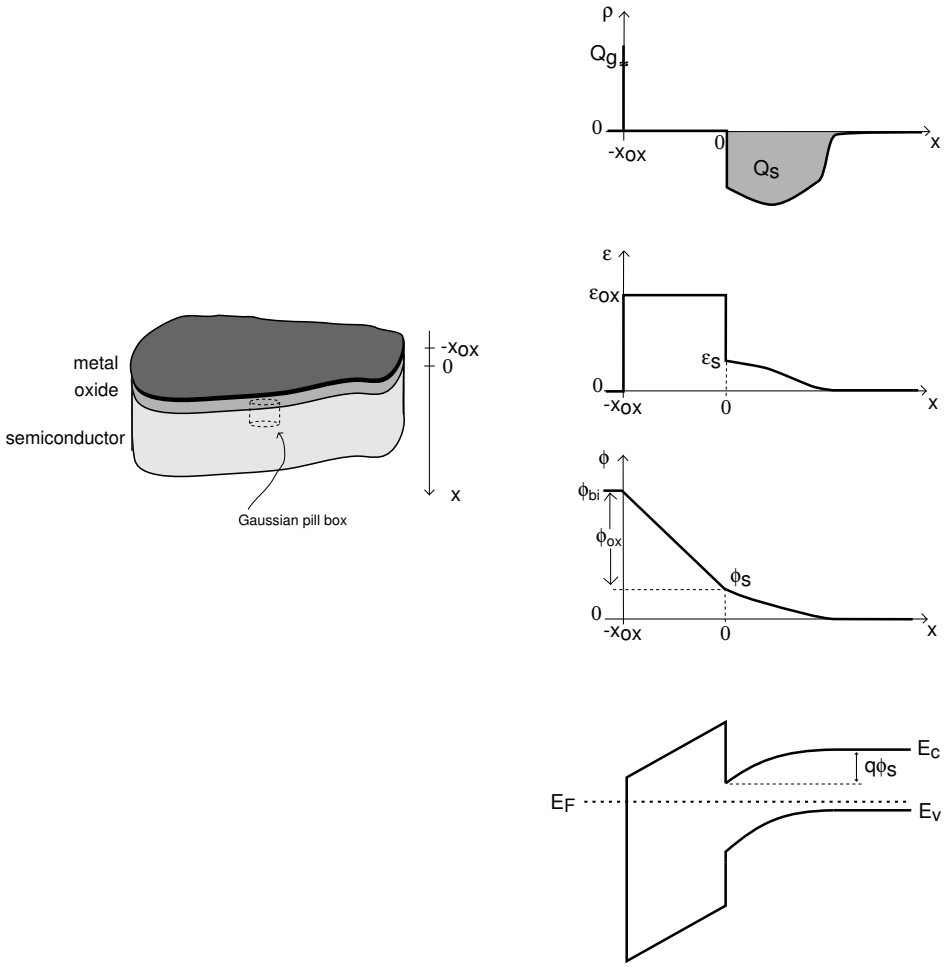
$$q\phi_{bi} = W_S - W_M$$

Note: large band discontinuities at insulator-semiconductor interface.

Other possible band arrangements depending on relative values of W_S and W_M:



□ General relations for MOS electrostatics



- no charge in dielectric
- overall charge neutrality:

$$Q_g = -Q_s$$

- field inside dielectric uniform:

$$\mathcal{E}_{ox} = -\frac{Q_s}{\epsilon_{ox}}$$

- normal component of displacement vector conserved at semiconductor/dielectric interface:

$$\epsilon_s \mathcal{E}_s = \epsilon_{ox} \mathcal{E}_{ox}$$

Hence field at semiconductor surface:

$$\mathcal{E}_s = -\frac{Q_s}{\epsilon_s}$$

Total potential difference across structure:

$$\phi_{bi} = \phi_s + \phi_{ox}$$

-drop across semiconductor, ϕ_s, called *surface potential*

-drop in oxide:

$$\phi_{ox} = x_{ox}\mathcal{E}_{ox}$$

Define *oxide capacitance per unit area*:

$$C_{ox} = \frac{\epsilon_{ox}}{x_{ox}}$$

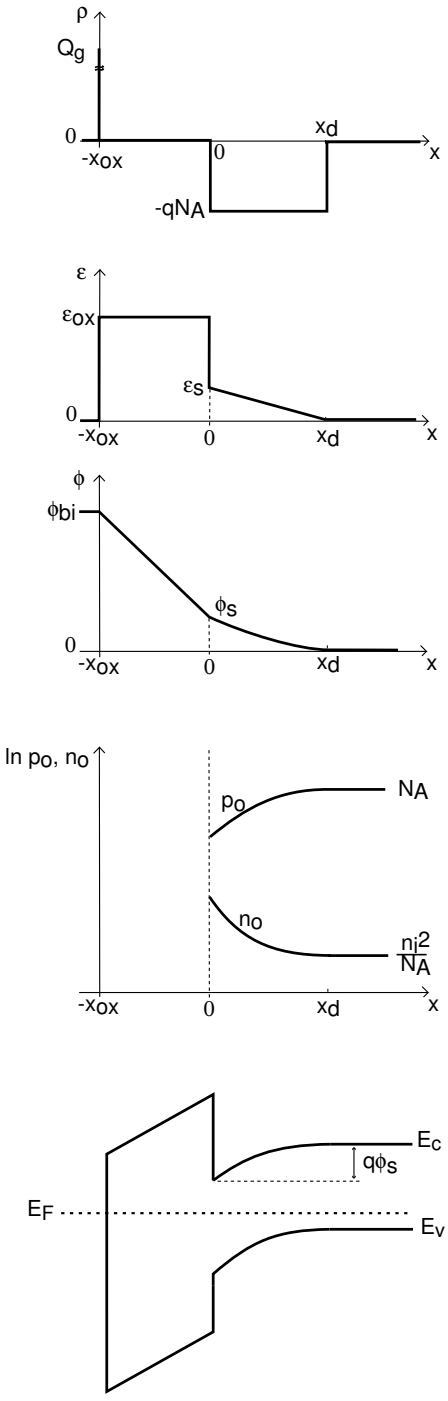
All together, total potential build-up across MOS:

$$\phi_{bi} = \phi_s - \frac{Q_s}{C_{ox}}$$

Key relationship between ϕ_s and Q_s.

□ Depletion

Do depletion approximation:



Integrated semiconductor charge:

$$Q_s \simeq -qN_A x_d$$

Field at semiconductor surface:

$$\mathcal{E}_s \simeq \frac{qN_A x_d}{\epsilon_s}$$

Field in insulator:

$$\mathcal{E}_{ox} \simeq \frac{qN_A x_d}{\epsilon_{ox}}$$

Surface potential:

$$\phi_s \simeq \frac{qN_A x_d^2}{2\epsilon_s}$$

Everything in terms of x_d, but don't know x_d!

Demand ϕ_{bi} be the right amount from energy considerations:

$$\phi_{bi} = \frac{1}{q}(W_S - W_M) = \phi_s + \phi_{ox} \simeq \frac{qN_A x_d^2}{2\epsilon_s} + \frac{qN_A x_d}{C_{ox}}$$

Solve for x_d:

$$x_d \simeq \frac{\epsilon_s}{C_{ox}}(\sqrt{1 + \frac{4\phi_{bi}}{\gamma^2}} - 1)$$

Where γ is *body-factor coefficient*:

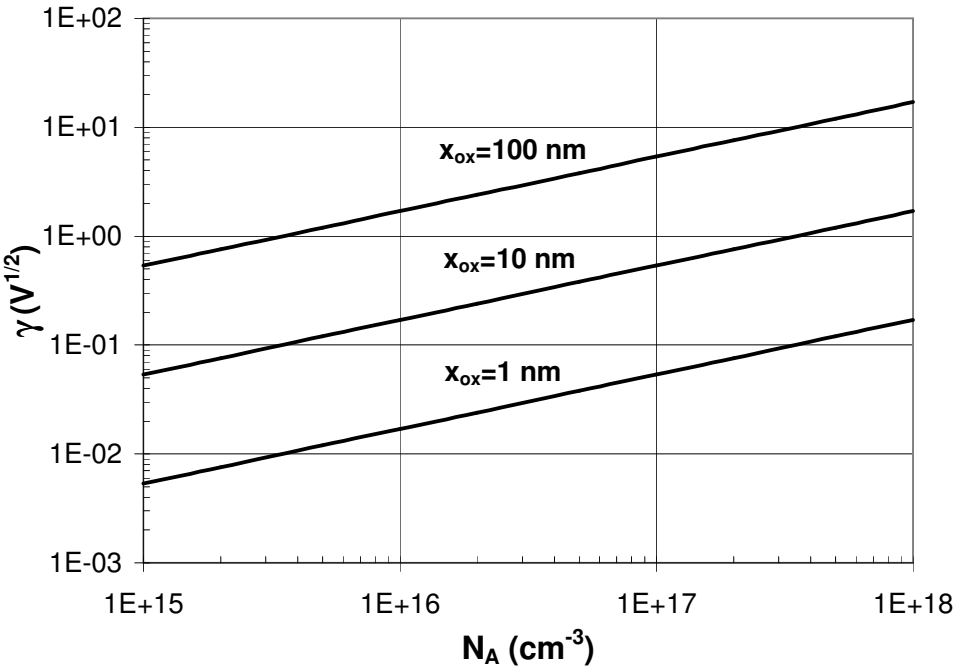
$$\gamma = \frac{1}{C_{ox}}\sqrt{2\epsilon_s q N_A}$$

Key dependencies: $\phi_{bi} \uparrow \rightarrow x_d \uparrow$

$$N_A \uparrow \rightarrow x_d \downarrow$$

Body-factor coefficient, γ:

$$\gamma = \frac{1}{C_{ox}}\sqrt{2\epsilon_s q N_A}$$



γ depends on:

- doping of body
- capacitance of insulator

$\Rightarrow$ relative magnitude of depletion capacitance and oxide capacitance.

In well designed MOSFETs, $\gamma \sim 0.1 - 1\ V^{1/2}$.

Key conclusions

- Si/SiO_2 interface nearly ideal: most Si bonds satisfied but interface about two monolayers rough.
- Most typical zero bias case of MOS structure: *depletion* region next to Si/SiO_2 interface; other possible cases: *accumulation* or *inversion*.
- *Surface potential*, ϕ_s: total potential build-up across semiconductor.
- General relationships for MOS electrostatics:
  - overall charge neutrality: $Q_g = -Q_s$
  - continuity of normal displacement vector at semiconductor/insulator interface: $\epsilon_s \mathcal{E}_s = \epsilon_{ox} \mathcal{E}_{ox}$
  - total potential difference must add up to ϕ_{bi}: $\phi_{bi} = \phi_s - \frac{Q_s}{C_{ox}}$
- Order of magnitude of key parameters of Si at 300K:
  - Body factor coefficient: $\gamma \sim 0.1 - 1\ V^{1/2}$ (depends on doping level of semiconductor and insulator capacitance).