

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
Department of Electrical Engineering and Computer Science

6.374: Analysis and Design of Digital Integrated Circuits
CAD Tutorial: An Introduction to Magic

Fall 2003

Issued: 9/10/03

CAD Tools for 6.374

We will use three CAD tools for 6.374: Magic, HSPICE and Nanosim.

Magic is used for drawing the layout of circuits. With the layout, we can perform extraction from layout to a HSPICE deck for simulation. The HSPICE deck contains information about the geometry of individual devices and parasitic capacitances of interconnects. It is similar to the HSPICE decks that you may use for the first problem set. This tutorial covers the basics of how to use Magic.

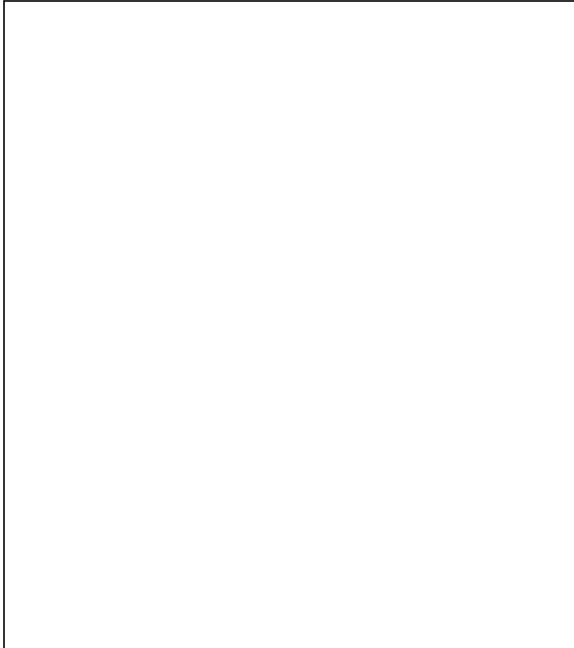
Magic Tutorial

Drawing a CMOS gate: 2-Input NAND

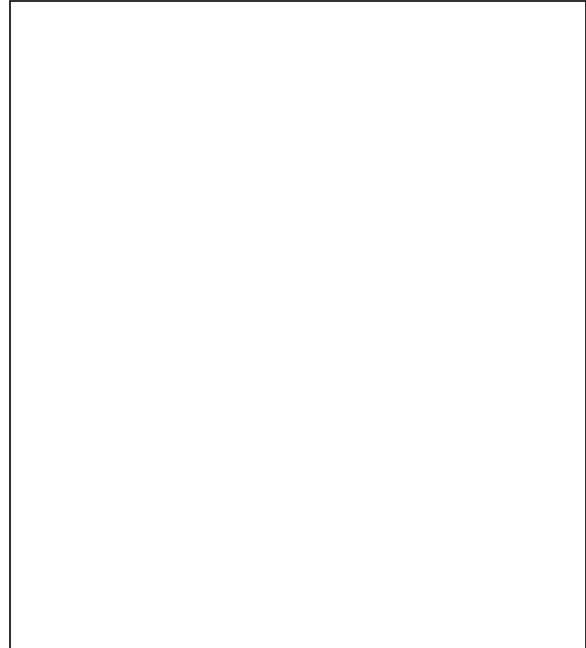
Task: Layout a 2-Input NAND gate with NMOS size 0.5/0.25 and PMOS size 0.75/0.25. Inputs should enter from the left in Poly and the output should exit the right in Poly. Power and Ground rails run vertically in Metal 1.

STEP 1: Plan your design.

In the space provided on the left, draw the circuit schematic for a 2-Input NAND gate. In the space on the right, sketch the layout for your design.



Sketch the Schematic



Sketch the Layout

STEP 2: Starting to Layout - Drawing the NFETs

When you start Magic, a window should appear as shown in Figure 1. This is where you will draw your layout. The window in which you started 'magic' now becomes the console and logs all the commands and macros you type. Always point your mouse in the drawing window when you type a command or macro.

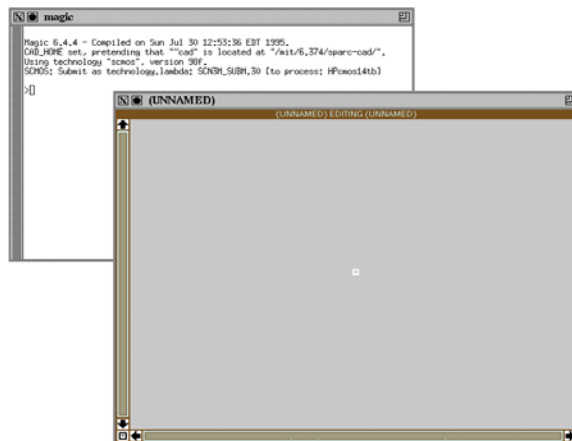


Figure 1: Magic window.

First, to facilitate your drawing, make the grid appear by typing 'g' (with the mouse in the drawing window.) You may not see the grid because the zoom is inappropriate. Type 'v' to zoom to the current selected object, which is a square. Type 'Z' to zoom out by a factor of 2 and 'z' to zoom in. The size of a small square is 1λ .

Doing layout involves drawing rectangles and painting them to represent various layers. We will now draw an n-channel MOSFET (the uppermost one in the pair). At any point, to undo a the last step, type 'u'.

Step 1: Drawing the source, drain and channel region.

Anchor one corner of a rectangle by clicking the left mouse button (in the Magic window). To select the other corner of the rectangle, click the right mouse button. (Make sure your mouse cursor looks like a cross-hair. If not, press space bar a few times until you see it.) Select a 17x4 rectangle. With the mouse in the window type (yes, include the ':')

```
:paint ndiff
```

You should see a green rectangle as shown in Figure 2

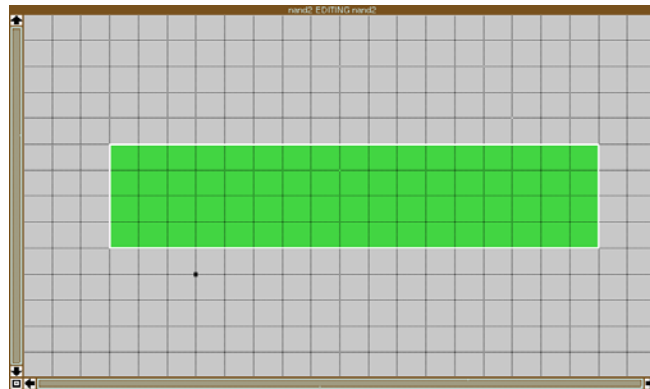


Figure 2: Source, drain and channel region

Step2: Drawing the poly gate

Using the same method, select a 2x8 rectangle overlapping the green rectangle. Type

```
:paint poly
```

Add a second rectangle of poly three boxes away from the first.

You should see two red rectangles overlapping the green rectangle as shown in Figure 3. The overlapping regions are the channels of our two NFET devices.

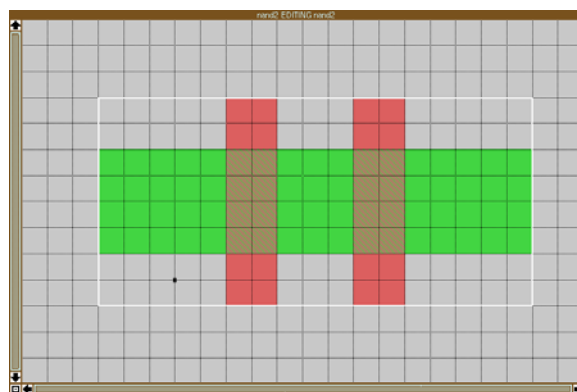


Figure 3: Poly gates over channel with source and drains on the side

Step 3. Drawing the M1 output contact

Select a 4x4 rectangle on the right side of the green rectangle. Type
`:paint ndc`

This is a metal to n-diffusion contact. You do not need a contact on the source because it abuts directly with the other NMOS device. Add a contact to the source of the second NMOS device (far left side).

Layer Names

The names of some various 'layers' are:

m1 - metal1
m2 - metal2
pdiff - p+ diffusion
pdc - p+ to metal 1 contact.
nwell - nwell for the p-channel MOSFET
nwc - nwell to metal1 contact
pwc - p substrate to metal1 contact
pc - poly to metal1 contact
m2c - metal1 to metal2 contact

Short-cuts for drawing

Instead of typing '`:paint ...`', once you have the basic layers on the drawing, you can copy and paste as follows. Select a rectangle. Point the mouse at a region in the drawing which has the color you want to paint the selected rectangle and click the middle button. To erase a certain rectangle, click the middle button with the mouse pointed on the background.

Breaking and fixing design rules

When design rules are broken, magic gives a warning by covering the rectangle which has violated design rules with an array of white dots.

In your drawing, select the tip of the poly and paint it gray. Type 'y' with the mouse in the dotted region to see what design rule has been violated. In this case, the console reads:

```
Poly overhang of Transistor < 2 (Mosis #3.3) [nfet,pfet space/  
active,poly,pres,rp,pc/a poly,pres,rp,pc/a]
```

Practice breaking and fixing a few design rules. And now, BACK TO THE NAND GATE....

STEP 3 - Drawing the PFETs

Now draw the two PFETs above the NFETs. Give yourself LOTS of space for wiring and for meeting design rules. To draw the PFETs, you will need to lay down an n-well, p-diffusion, poly, and contacts. Is the location of the contacts the same as for the NFETs?

Figure 4 shows the layout with all four FETs in place.

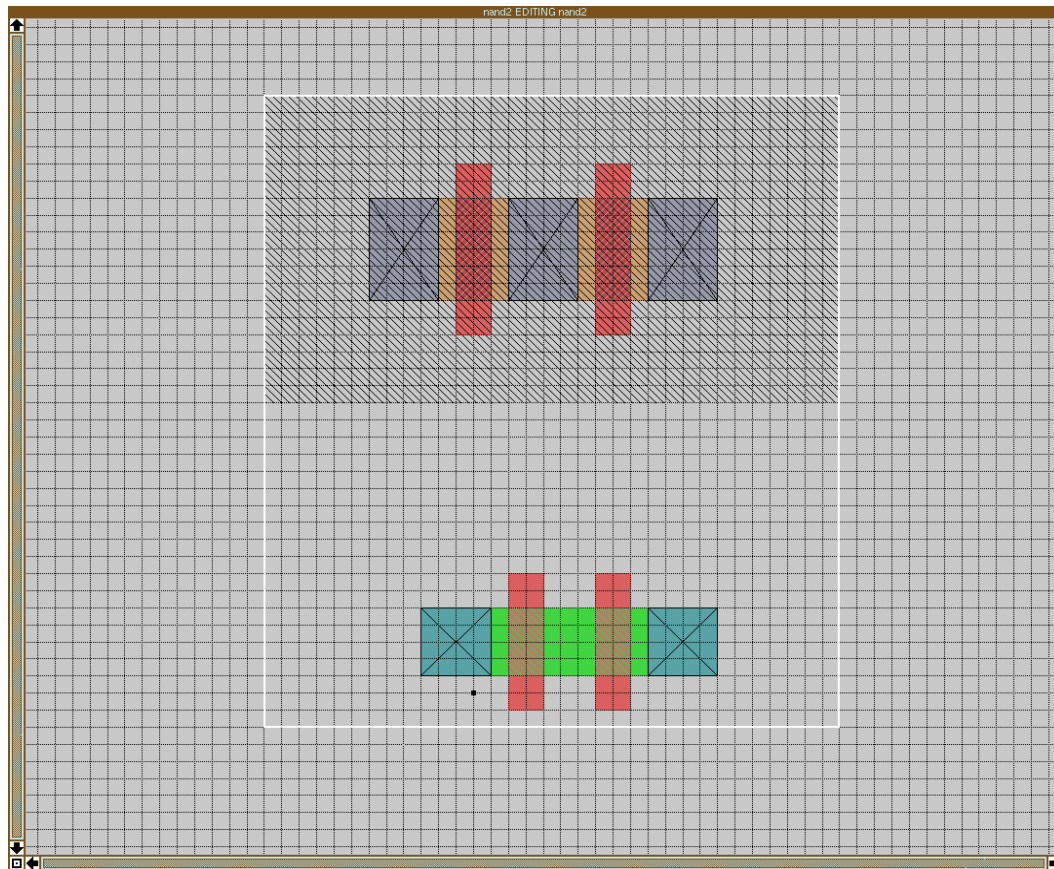


Figure 4: Four FETs (2 parallel PMOS, 2 series NMOS)

STEP 4 - Wiring up the NAND gate

To connect metal to a via, just draw metal touching the via. For example, select a rectangle of at least 3x3 touching any contact. Type

```
:paint m1
```

This paints a layer of metal 1.

Wire up the gates of the FETs in poly. You will have to jumper one of the gates in metal1 to bring poly out to the left of the design. Now wire up the output node. Remember that you want to minimize capacitance at this node. Now wire up the power and ground. Are all of the connections in the circuit complete?

NO! You need to make contacts for the body terminals of your devices. Find the right type of contact in the layer list, and add the well contacts to your design.

STEP 5 - Labeling your circuit

Once you have drawn your circuit, you need to label the ports so that you can do an extraction of the layout into a circuit, including geometrical information and parasitics.

Click the middle of the VDD power strip with the left mouse button, followed by the right mouse button.

Type

```
:label VDD!
```

A label for VDD! appears. Do the same for the other nodes in the circuit.

You should get something like Figure 5 for your final layout. If you want to erase a label, select a rectangle containing the label and type

```
:erase label
```

Note: The '!' in 'VDD!' represents that it is a global signal. It is the same when used in all instances. (Refer to the section on hierarchical designs about making instances of cells.)

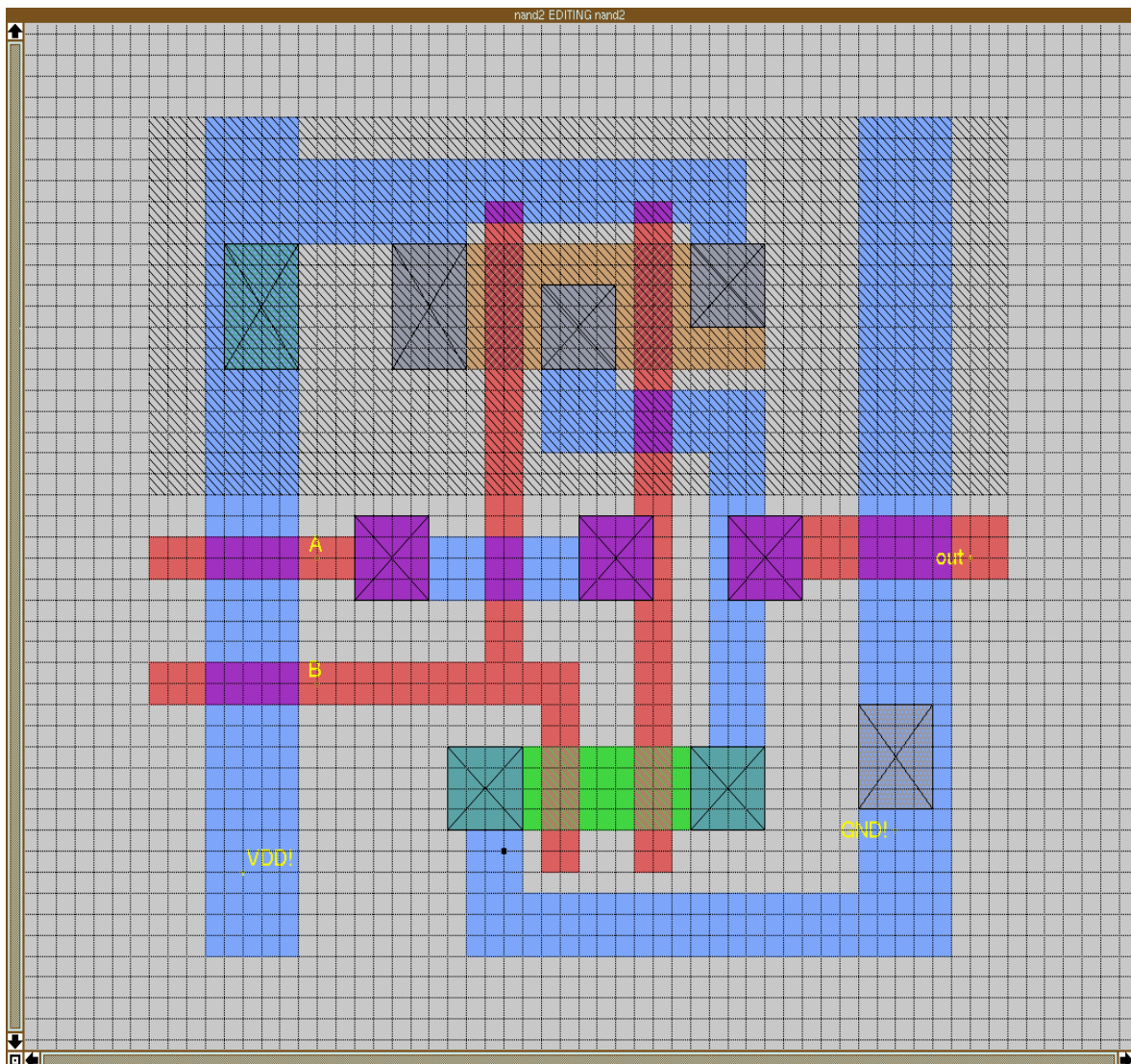


Figure 5: NAND gate complete with labels

STEP 6 - Saving, loading and extracting

To save, type
`:save tutorial`

To load, type
`:load tutorial`

To extract the layout into a circuit for simulation in HSPICE and Irsim, type
`:extract`

This will create a file `tutorial.ext` which can be converted into a HSPICE deck and Nanosim deck using `ext2spice` and `ext2sim` respectively. We will discuss this later.

You can type
`:quit`
to exit Magic.

STEP 7 - Creating and Verifying your netlist

Convert the layout to a spice netlist. View the netlist to see if it looks correct.

Are there any problems?

You will find that CAD tools **never** do everything you would like. For example, the netlist sizes devices in terms of a scaled unit, but it uses the wrong scale unit! Also, the names of the FETs are `nfet` and `pfet`, not `nch` and `pch`. VLSI designers become masters at writing scripts to tie together CAD tools and to make things work.

More short cuts for drawing

Selecting and Moving

You may want to move certain blocks. To select a rectangle, point the mouse over the rectangle and type 's'. To select a whole region, select a rectangle, and type 'a'

Once a rectangle or block is selected, you can move them by typing 'q' for left, 'w' for down, 'e' for up and 'r' for right.

Hierarchy in designs

In the layout of complex circuits, hierarchy is very useful to maintaining modularity. For example, an 8-bit adder can be made from an array of 1 bit adders. However, to be able to do this, it is necessary to layout cells so that they can be made into modules by putting them next to each other.

Here is an example of how to create an array of cells:

```
:getcell name
```

finds the file `name.mag` on disk, reads the cell it contains, and creates an instance of that cell.

To turn the instance into an array, invoke the command:

```
:array xsize ysize
```

where *xsize* and *ysize* indicates how many elements the array should have in the x- and y-direction respectively.

To see the layout in individual cells, use the command `:expand all`.

Here is how to generate an array of your nand gate:

Step 1. Layout the nand gate and save it with a name like 'tutorial'..

Step 2. Use the command `:getcell tutorial` to create an instance of the nand gate.

Step 3. Use the command `:array 3 1` to make an array 3 by 1 of the gate.

Step 4. Use the `:expand` to display the layout of each cell.

You probably would need to modify the original cell so that the inputs and outputs meet up correctly.