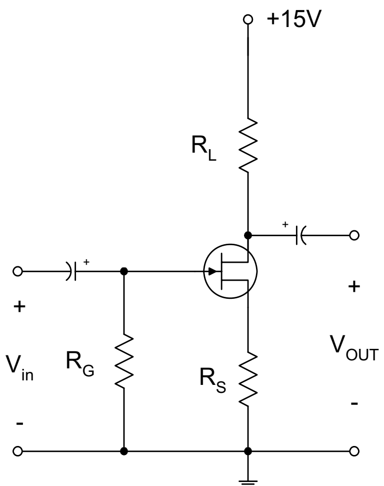
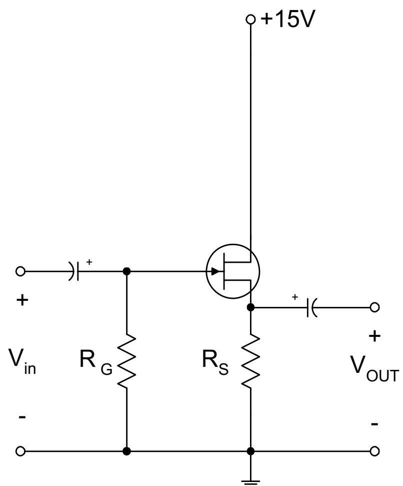
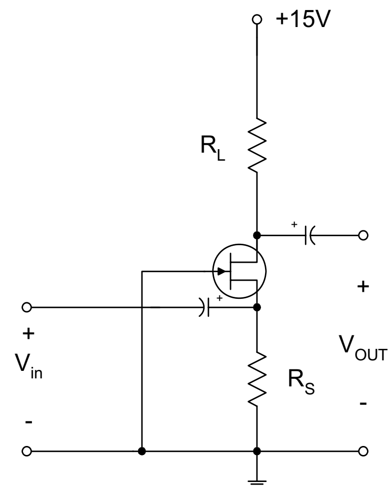
JFET AMPLIFIER CONFIGURATIONS



[a] Common Source Amplifier



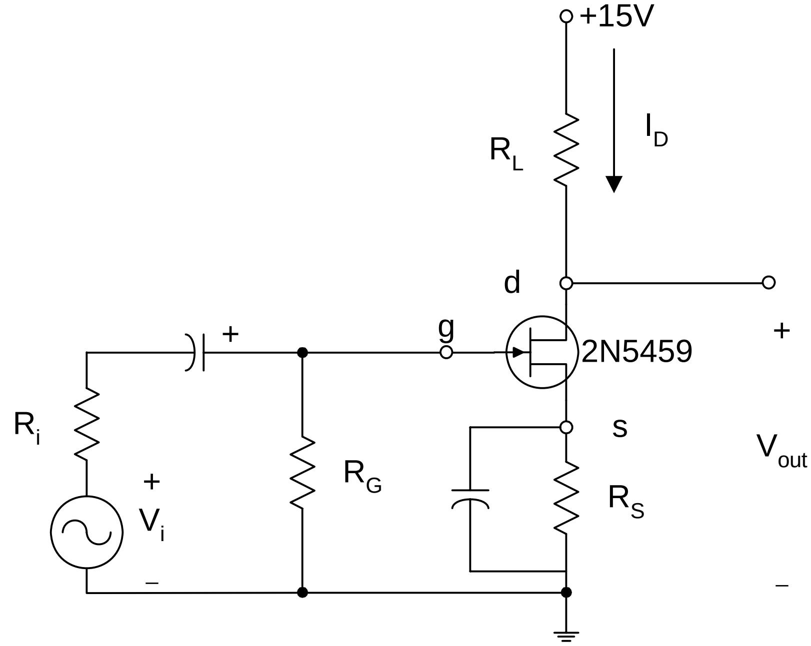
[b] Common Drain [Source Follower] Amplifier

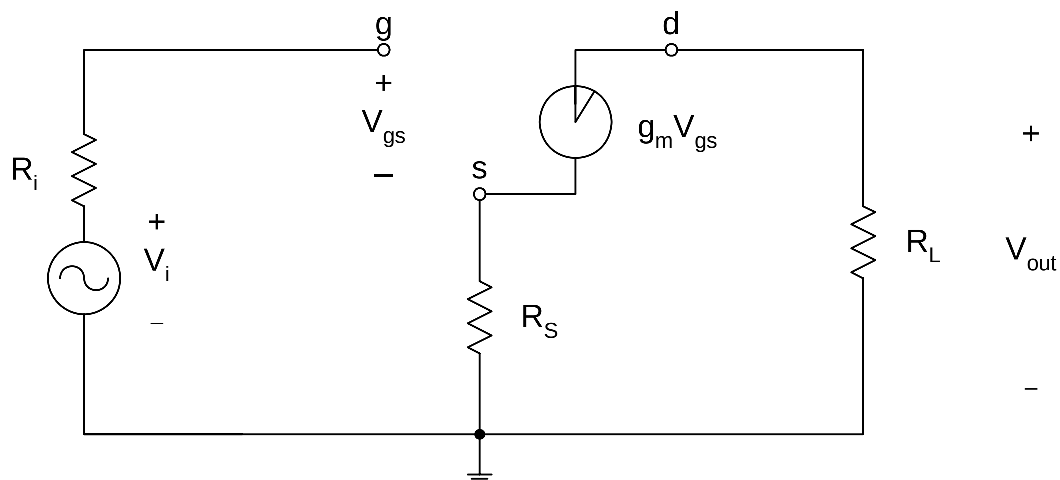


[c] Common Gate Amplifier

JFET AMPLIFIER CONFIGURATIONS WITH HYBRID-Π EQUIVALENT CIRCUITS

COMMON SOURCE AMPLIFIER WITH BYPASSED SOURCE RESISTOR



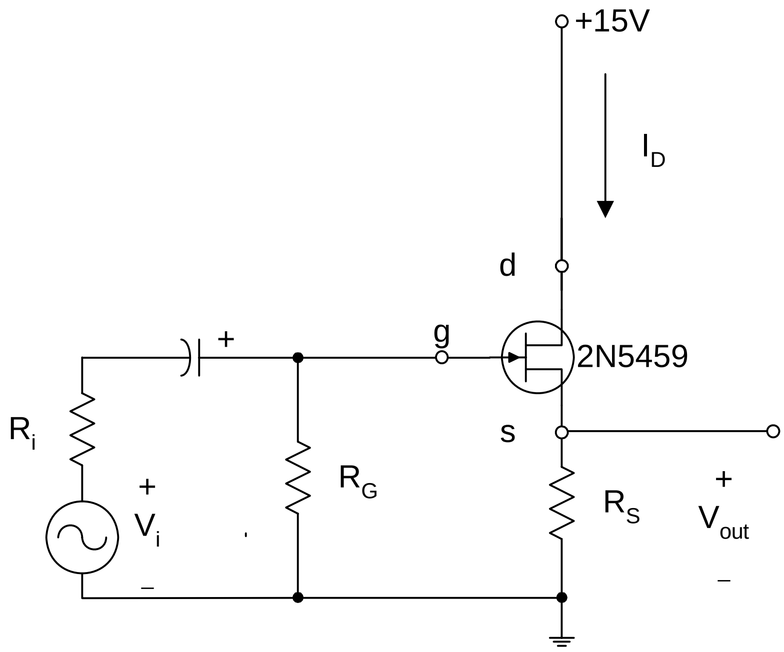


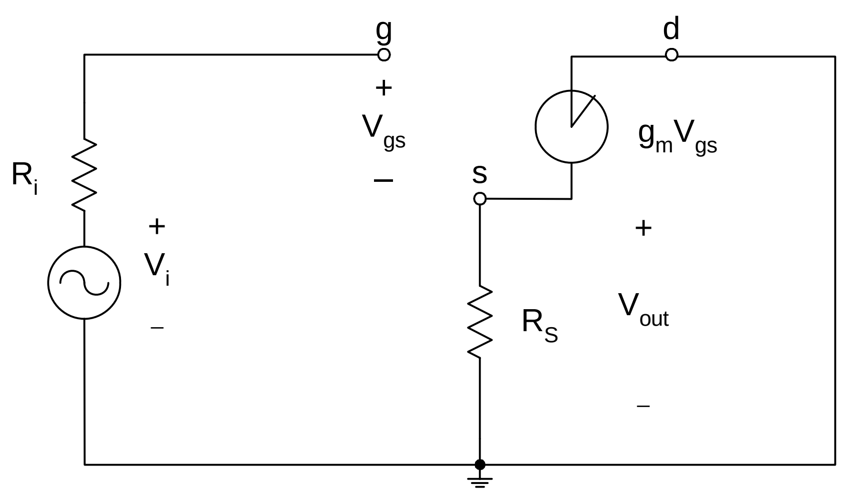
$$A_v = \frac{v_{out}}{v_{in}} = \frac{-g_m v_{gs} R_L}{v_{gs} + g_m v_{gs} R_S} = \frac{-g_m v_{gs} R_L}{v_{gs}[1 + g_m R_S]}$$

$$A_v = \frac{-g_m R_L}{1 + g_m R_S} \qquad or \qquad A_v = -g_m R_L$$

JFET AMPLIFIER CONFIGURATIONS WITH HYBRID-Π EQUIVALENT CIRCUITS

COMMON DRAIN [SOURCE FOLLOWER] AMPLIFIER

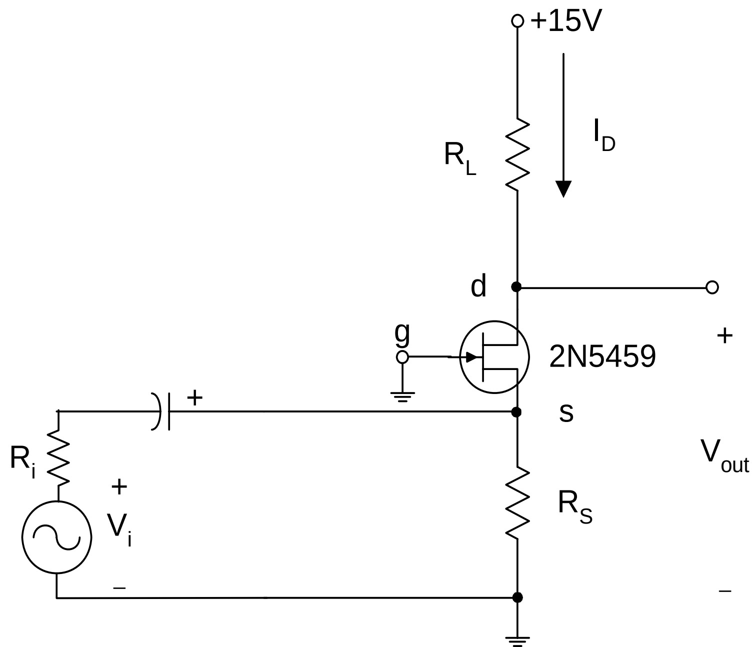


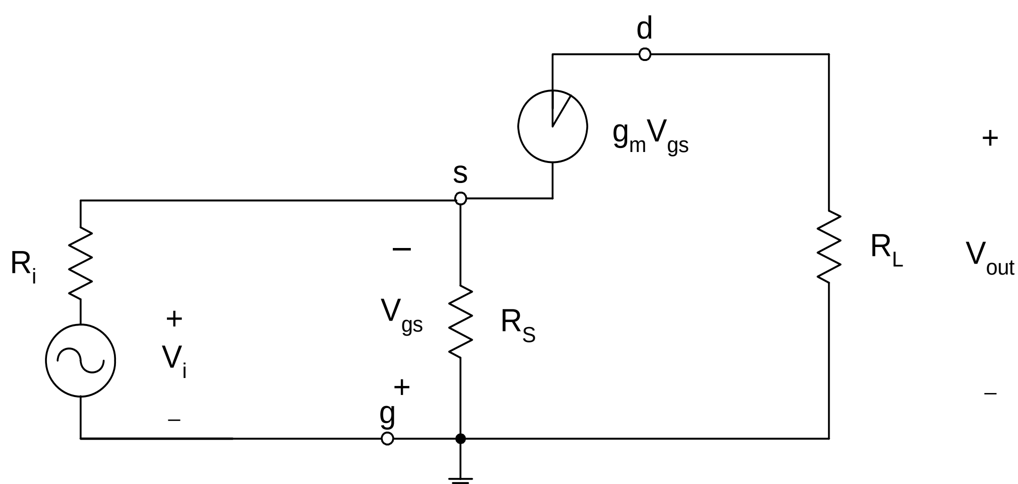


$$A_v = \frac{v_{out}}{v_{in}} = \frac{g_m v_{gs} R_S}{v_{gs} + g_m v_{gs} R_S} = \frac{g_m v_{gs} R_S}{v_{gs}\left[1 + g_m R_S\right]}; \qquad A_v = \frac{g_m R_S}{1 + g_m R_S}$$

JFET AMPLIFIER CONFIGURATIONS WITH HYBRID-Π EQUIVALENT CIRCUITS

COMMON GATE AMPLIFIER





$$A_v = \frac{v_{out}}{v_{in}} = \frac{-g_m v_{gs} R_L}{-v_{gs}\left[g_m R_i + \frac{R_i}{R_S} + 1\right]} = \frac{g_m R_L}{1 + g_m R_i + \frac{R_i}{R_S}}; \quad if \;\; R_i = 0,$$

$$then \quad A_v = g_m R_L$$

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Low Frequency Hybrid-π Equation Chart

TRANSISTORS

Characteristic	**Common Emitter**	**CE with R_E**	**CC [E. Follower]**	**Common Base**
Voltage Gain [if $r_o >> R_L$]	$A_v = -g_m R_L$	$A_v \approx -\frac{R_L}{R_E}$	$A_v \approx 1$	$A_v = \frac{\beta_o R_L}{r_\pi // R_E + (\beta_o + 1) R_s}$
Current Gain	β_o	β_o	$\beta_o + 1$	$\frac{\beta_o}{\beta_o + 1}$
Input Impedance	$r_\pi // R_B$	$[r_\pi + (\beta_o + 1) R_E] // R_B$	$[r_\pi + (\beta_o + 1) R_E] // R_B$	$\frac{r_\pi}{\beta_o + 1}$
Output Impedance	R_L [if $r_o >> R_L$]	R_L [if $r_o >> R_L$]	$\left[\frac{(r_\pi + R_s // R_B)}{\beta_o + 1}\right] // R_E$	R_L [if $r_o >> R_L$]
Phase Reversal?	Yes	Yes	No	No

JFET'S

Characteristic	**Common Source**	**C Source with R_S**	**Common Drain [Source Follower]**	**Common Gate**
Voltage Gain [if $r_{ds} >> R_L$]	$A_v = -g_m R_L$	$A_v = \frac{-g_m R_L}{1 + g_m R_S}$	$A_v = \frac{g_m R_S}{1 + g_m R_S}$	$A_v = \frac{g_m R_L}{1 + g_m R_i + \frac{R_i}{R_S}}$ R_i = generator resistance
Current Gain	$\frac{I_D}{I_S}$ Very large!	$\frac{I_D}{I_S}$ Very large!	$\frac{I_D}{I_S}$ Very large!	$A_i = \frac{g_m R_S}{g_m R_S + 1}$
Input Impedance	R_G	R_G	R_G	$\frac{R_S}{g_m R_S + 1} = \frac{1}{g_m} // R_S$
Output Impedance	R_L [if $r_{ds} >> R_L$]	R_L [if $r_{ds} >> R_L$]	$\frac{R_S}{g_m R_S + 1} = \frac{1}{g_m} // R_S$	R_L [if $r_{ds} >> R_L$]
Phase Reversal?	Yes	Yes	No	No

FET COMMON-SOURCE AMPLIFIER BIASING-GRAPHICAL METHOD #1

1. FIND $V_{GS(OFF)}$ & I_{DSS} FOR YOUR DEVICE; MEASURE USING CURVE TRACER. [$V_{GS(OFF)}$ = GATE-SOURCE VOLTAGE FOR WHICH $I_D = 0$. $I_{DSS} = I_D$ WHEN $V_{GS} = 0$]
2. ASSUME $R_S << R_L$.
3. PLOT A LOAD LINE ON THE OUTPUT CHARACTERISTICS. KEEP THE I_D , $V_{DS} = 0$ INTERCEPT ON THE GRAPH PAGE; I. E. STAY AWAY FROM NEARLY VERTICAL LOAD LINES.
4. CALCULATE R_L FROM THE LOAD LINE INTERCEPTS. USE CLOSEST STD. VALUE.
5. PICK Q-POINT VALUE OF V_{GS} FOR MAXIMUM LINEAR OUTPUT SWING.
6. CALCULATE I_D: $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$; OR ESTIMATE FROM CHARACTERISTICS.
7. CALCULATE R_S FOR V_{GS} AT I_D . $\left(R_S = \frac{V_{GS}}{I_D}\right)$. USE CLOSEST STANDARD VALUE.
8. COMPARE R_S AND R_L ; IF R_S IS CLOSE TO R_L , REPLOT THE LOAD LINE.
9. RECALCULATE R_S FOR NEW V_{GS} . REPEAT STEPS 7 AND 8 AS NECESSARY!

CALCULATING JFET SMALL-SIGNAL g_m

1. CALCULATE g_m FROM $\Delta I_D / \Delta V_{GS}$ ON DRAIN CHARACTERISTICS FROM CURVE TRACER [LARGE SIGNAL g_m]

   2. OR USE MEDIAN SPECIFICATION SHEET VALUE. [FOR A FAST ESTIMATE.]

OR $$g_m = \frac{-2I_{DSS}}{V_{GS(off)}}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right) = \frac{-2I_{DSS}}{V_{GS(off)}}\sqrt{\frac{I_D}{I_{DSS}}}$$ WHERE V_{GS} or I_D = OPERATING POINT.

When $V_{GS} = V_{GS(OFF)}$, $I_D = 0$; $I_{DSS} = I_D$ @ $V_{GS} = 0$. NOTE THAT THE SMALL-SIGNAL

TRANSCONDUCTANCE DEPENDS ON THE DC BIAS POINT, JUST AS IT DOES FOR THE BIPOLAR TRANSISTOR!

FET COMMON-SOURCE AMPLIFIER BIASING-GRAPHICAL METHOD #2

1. FIND $V_{GS(OFF)}$ & I_{DSS} FOR YOUR DEVICE; MEASURE USING CURVE TRACER. [$V_{GS(OFF)}$ = GATE-SOURCE VOLTAGE FOR WHICH $I_D = 0$. $I_{DSS} = I_D$ WHEN $V_{GS} = 0$]

2. REFER TO THE COMBINED TRANSFER [TRANSCONDUCTANCE] CHARACTERISTICS AND DRAIN CHARACTERISTICS CURVES [ATTACHED].

3. CHOOSE R_S AS FOLLOWS: $R_S = \left|\frac{V_{GS(OFF)}}{I_{DSS}}\right|$. DRAW THE LINE REPRESENTING R_S FROM THE ORIGIN OF THE TRANSFER CURVE GRAPH; THE “Q” POINT IS AT THE INTERSECTION OF THE TWO PLOTS. THIS SETS I_{DQ} AT ABOUT 0.4 I_{DSS}.

4. EXTEND A HORIZONTAL LINE FROM THE I_{DQ} VALUE ON THE TRANSFER CHARACTERISTICS’ LEFT-HAND AXIS ALL THE WAY ACROSS THROUGH THE DRAIN CHARACTERISTICS.

5. THE RIGHT-HAND VOLTAGE INTERCEPT FOR THE LOAD LINE [ON THE DRAIN CHARACTERISTICS] IS EQUAL TO THE SUPPLY VOLTAGE V_{DD}. CHOOSE A VALUE FOR V_{DSQ} THAT GIVES A ROUGHLY SYMMETRICAL OUTPUT VOLTAGE SWING AROUND V_{DSQ}.

6. DRAW A VERTICAL LINE FROM V_{DSQ} UPWARDS TO INTERSECT WITH THE LINE DRAWN IN STEP #4. THIS INTERSECTION GIVES THE Q-POINT.

7. DRAW THE LOAD LINE FROM THE SUPPLY VOLTAGE THRU THE Q-POINT UNTIL IT INTERSECTS WITH THE CURRENT AXIS.

8. DIVIDE THE SUPPLY VOLTAGE BY THE CURRENT AXIS VALUE TO GET THE TOTAL VALUE OF RESISTANCE IN THE DRAIN-SOURCE CIRCUIT.

9. SUBTRACT THE VALUE OF R_S FOUND IN STEP #3 FROM THE VALUE FOUND IN STEP #8 TO GET THE VALUE OF LOAD [OR DRAIN] RESISTOR. USE CLOSEST STANDARD VALUE FOR BOTH RESISTORS.

10. NOTE THAT THE MORE VERTICAL THE LOAD LINE, THE SMALLER THE VALUE OF R_L. LOW R_L EQUALS LOW VOLTAGE GAIN [$A_V = - g_m R_L$]. ACCEPTING A LOWER VOLTAGE V_{DQ} WITH ITS ATTENDANT ASYMMETRICAL VOLTAGE SWING WILL ALLOW A HIGHER VALUE R_L. INCREASING SUPPLY VOLTAGE WILL ALSO ALLOW A LARGER VALUE OF R_L AND A MORE SYMMETRICAL VOLTAGE SWING. [THE MORE HORIZONTAL THE LOAD LINE, THE HIGHER THE TOTAL DRAIN-SOURCE RESISTANCE.]

FET SOURCE-FOLLOWER LOAD LINE/GAIN EXAMPLES & METHOD

1. FIND $V_{GS(OFF)}$ & I_{DSS} FOR YOUR DEVICE; MEASURE USING CURVE TRACER. [$V_{GS(OFF)}$ = GATE-SOURCE VOLTAGE FOR WHICH $I_D = 0$. $I_{DSS} = I_D$ WHEN $V_{GS} = 0$]

2. CHOOSE Q-POINT; i.e. CHOOSE $-V_{GS}$ FROM DRAIN CHARACTERISTICS GRAPH.

3. CALCULATE I_D: $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$; OR ESTIMATE FROM CHARACTERISTICS.

4. CALCULATE R_S; USE CLOSEST STANDARD VALUE.

5. CALCULATE LOAD LINE INTERCEPTS, [MAY HAVE TO USE Δ BECAUSE THE I_D-V_{DS} = 0 INTERCEPT MAY BE WAY OFF THE GRAPH PAGE].

6. CALCULATE g_m:
$$g_m = \frac{-2I_{DSS}}{V_{GS(off)}}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right) = \frac{-2I_{DSS}}{V_{GS(off)}}\sqrt{\frac{I_D}{I_{DSS}}}$$

7. CALCULATE A_v:
$$A_v = \frac{g_m R_S}{1 + g_m R_S}$$

8. $$R_o = \frac{1}{g_m} // R_S$$

9. EXAMPLES [$V_P = V_{GS(OFF)} = -5.8V$; $I_{DSS} = 9mA$]

	Example 1	Example 2	Example 3
1. V_{GS}, I_D	-4V, 1.2mA	-3V, 2.3mA	-2V, 4.2mA
2. R_S=	3.3 kΩ	1.2 kΩ	470 Ω
3. ΔI_D @ ΔV_{DS}	4.55mA	12.5V, 5.32mA	10V, 4.17mA
4. g_m=	963 μMHO	1,500 μMHO	2,030 μMHO

5. A_v=	.761	.643	.488
6. R_o=	790Ω	428Ω	240Ω